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# APPLICATION NOTE

## **ABSTRACT**

Different suppliers have introduced single-, dual-, and triple-gate devices, with many different names. This application note discusses the different call-outs for the various packages and provides the reader with a comparison of the drawings from different vendors.

## **AN10161**

### **PicoGate Logic footprints**

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2002 Oct 29

## PicoGate Logic footprints

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Most major Logic suppliers have added a new dimension to the standard logic package landscape with the introduction of the single-, dual- and triple-gate devices. These small packages are designated by many different names.

Philips Semiconductors calls their family PicoGate Logic™; Texas Instruments calls their family TinyLogic; Fairchild dubbed them Little Logic; ST calls theirs Single gate; ON Semiconductor calls their family MiniGate; Toshiba uses the moniker LMOS.

Trying to cross all of these families to a common package has become quite a chore. Suppliers have different names for their package outlines. There are 5-pin, 6-pin and 8-pin packages and each pin count is available with two different lead pitch options. The remainder of this paper will attempt to sort out the different call-outs for the various packages and provide the reader with a comparison of the drawings from different vendors.

### The 5-pin packages

Depending on the vendor, the 5-pin 0.65 mm lead pitch package is known as MO-203, SC70, SC70-5, SC88A, SOT323, SOT353, SSOP-5-P-0.65A or USV. Figure 1 shows the general package outline and a table of the various dimensions. So despite all of the different names used, all of the packages are footprint compatible.

For the 5-pin 0.95 mm lead pitch package, much the same can be said. Depending on the vendor, the package is referenced as a SOT753, SC74A, SC59, SOT23, SOT23-5, MO178, TSOP5 and SMV. Figure 2 shows the general package outline for the 0.95 mm pitch package and a table of the various dimensions. Again, it can easily be shown that even though tolerances vary slightly, all of the parts are footprint compatible.

### The 6-pin packages

The 6-pin package drawings have the same dimensions as the 5-pin package but have a 6<sup>th</sup> lead, so there are 3 pins on each side of the package. Philips, Fairchild and TI offer some single- and dual-gate devices in this package option. Fairchild differentiates the package by changing the package designator to P6X or M6X for the 0.65 and 0.95 mm pitch packages. However, Philips and TI use the same package designator as for the 5-pin package. ON Semiconductor and Toshiba do not offer a 6-pin device.

### The 8-pin packages

Dual- and triple-gate logic functions are offered by Toshiba, Philips, TI and Fairchild and use an 8-pin package. As with the 5- and 6-pin packages, there are also two different lead pitches available. The 0.65 mm lead pitch package from Toshiba calls it an SSOP-8-P-0.65. Philips calls it a SOT505-2. TI calls it an SM8, and Fairchild doesn't offer the package. The smaller 8-pin package uses a 0.5 mm lead pitch and is known as the US8 or VSSOP8. Philips, Toshiba, Fairchild and TI offer this smaller package. Figures 3 and 4 are the package outline drawings.

While the package naming convention is not as straightforward as some of the more standard 14-, 16- and 20-pin package options, these smaller footprint packages are sourced by multiple vendors whose package footprints are all compatible with each other. The larger 0.95 mm lead pitch offers some space savings over the more conventional TSSOP package while it allows the use of low cost PC board etching techniques. Where the ultimate space savings is required, users have the option to shifting to a 0.65 or 0.5 mm pitch package.

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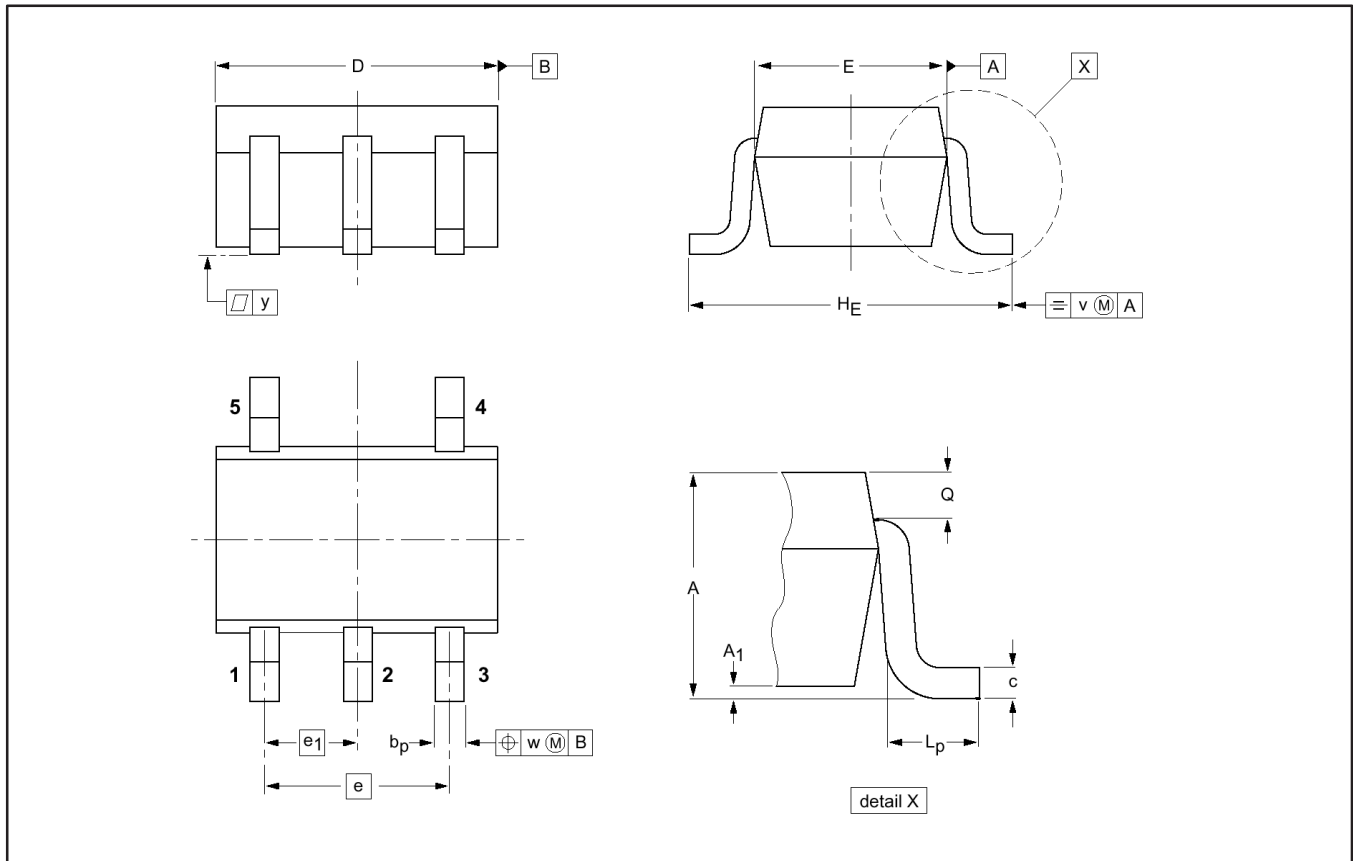


Figure 1. General package outline for a 5-pin 0.65 mm lead pitch package

All dimensions are in mm and are listed at the nominal value on the package drawing.

Table 1. 5-pin / 6-pin 0.65 mm lead pitch

Package	Dimension											Package designator
	A	A <sub>1 max</sub>	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	y	
SOT353 Philips	0.95	0.1	0.25	0.175	2.0	1.25	1.3	0.65	2.1	0.3	0.1	GW
SC70 T.I.	0.95	0.1	0.25	0.130	2.0	1.25	1.3	0.65	2.0	0.31	0.15	DCK
SC88A FCS	0.95	0.1	0.20	0.175	2.0	1.25	1.3	0.65	2.1	0.25	0.1	P5X/P6X
SOT323 ON	1.00	0.1	0.20	0.175	2.0	1.25	1.3	0.65	2.1	0.2	0.1	DFT
USV Toshiba	0.90	0.1	0.20	0.150	2.0	1.25	1.3	0.65	2.1	N/A	0.1	FU

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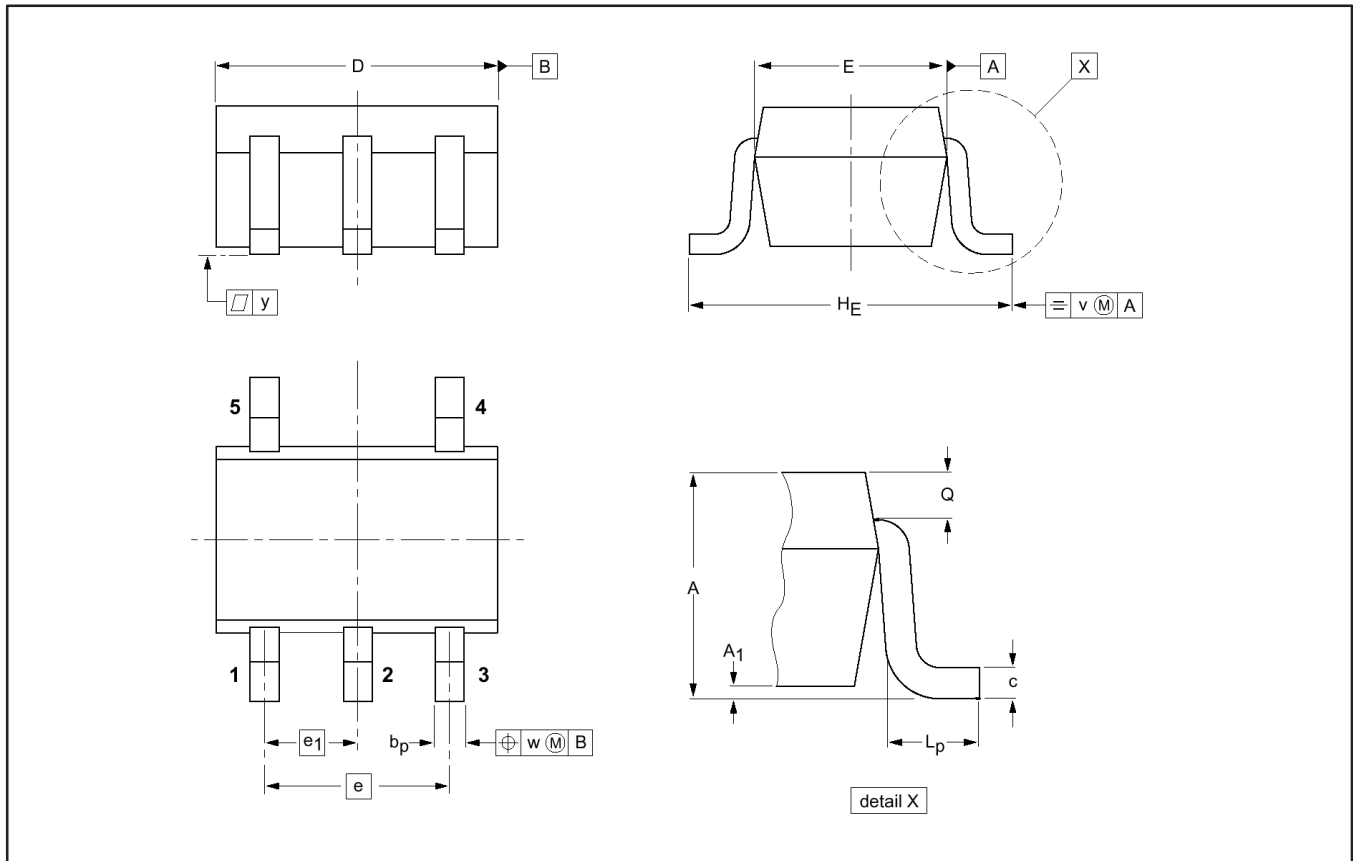


Figure 2. General package outline for a 5-pin 0.95 mm lead pitch package

All dimensions are in mm and are listed at the nominal value on the package drawing.

Table 2. 5-pin / 6-pin 0.95 mm lead pitch

Package	Dimension										Package designator
	A	A <sub>1 max</sub>	b <sub>p</sub>	c	D	E	e	H <sub>E</sub>	L <sub>p</sub>	y	
SOT753 Philips	1.000	0.10	0.325	0.180	2.9	1.5	0.95	2.75	0.40	0.10	GV
SOT23 T.I.	1.200	0.10	0.400	0.150	2.9	1.6	0.95	2.80	0.45	0.05	DBV
SOT23 FCS	1.175	0.10	0.400	0.140	2.9	1.6	0.95	2.80	0.45	0.10	M5X/M6X
SOT59-5 ON	1.000	0.10	0.375	0.175	3.0	1.5	0.95	2.75	0.40	0.05	DDT1
SMV Toshiba	1.100	0.10	0.400	0.160	2.9	1.6	0.95	2.80	N/A	0.10	F

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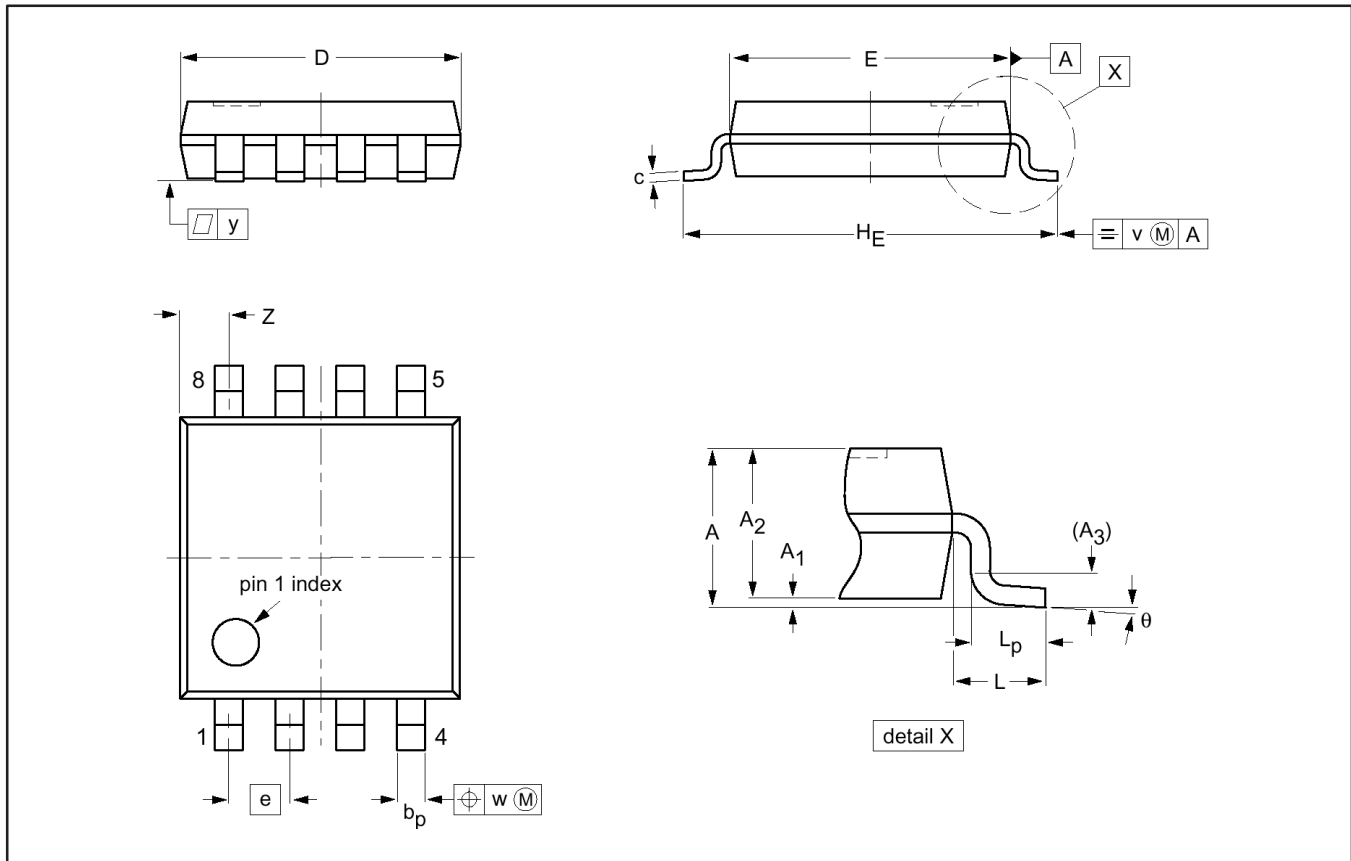


Figure 3. General package outline for an 8-pin 0.65 mm lead pitch package

All dimensions are in mm and are listed at the nominal value on the package drawing.

Table 3. 8-pin 0.65 mm lead pitch

Package	Dimension										Package designator
	A	A <sub>1 max</sub>	b <sub>p</sub>	c	D	E	e	H <sub>E</sub>	L <sub>p</sub>	y	
SOT505-2 Philips	1.100	0.15	0.280	0.130	3.00	3.00	0.65	4.00	0.40	0.10	DP
SM8 T.I.	1.300	0.10	0.225	0.150	2.95	2.80	0.65	4.00	0.40	0.10	DCT
SSOP8-P-0.65 Toshiba	1.100	0.50	0.200	0.150	2.90	2.90	0.65	4.00	N/A	0.10	FU

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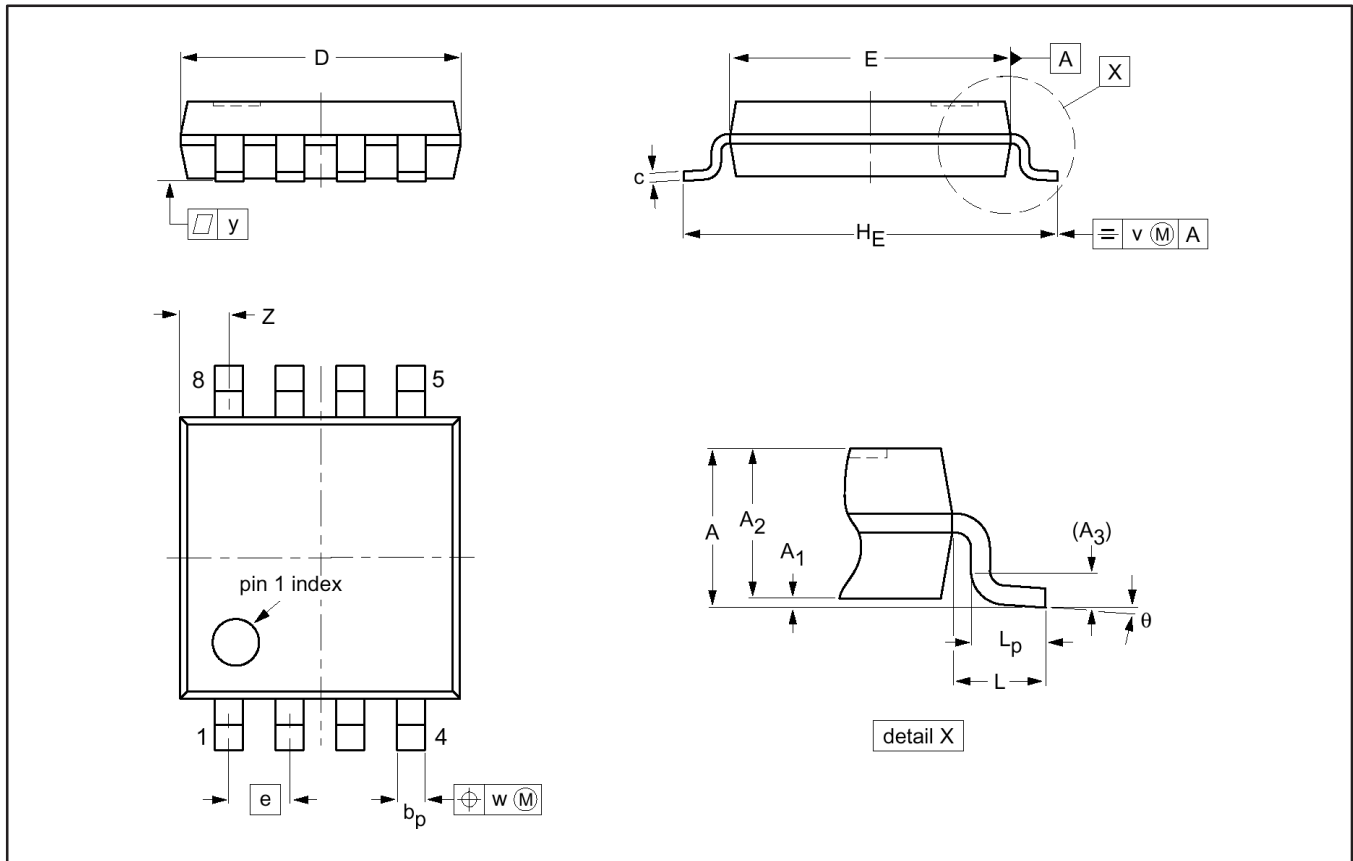


Figure 4. General package outline for an 8-pin 0.50 mm lead pitch package

All dimensions are in mm and are listed at the nominal value on the package drawing.

Table 4. 8-pin 0.50 mm lead pitch

Package	Dimension										Package designator
	A	A <sub>1 max</sub>	b <sub>p</sub>	c	D	E	e	H <sub>E</sub>	L <sub>p</sub>	y	
SOT765 Philips	1.000	0.15	0.220	0.140	2.00	2.20	0.50	3.10	0.275	0.10	DC
US8 T.I.	0.900	0.10	0.210	0.130	2.00	2.30	0.50	3.10	0.275	0.10	DCU
US8 Fairchild	0.900	0.10	0.220	0.130	2.00	2.30	0.50	3.10	0.275	0.10	K8X
VSSOP8 Toshiba	0.700	0.10	0.200	0.120	2.00	2.30	0.50	3.10	N/A	0.10	FK
US8 ON	0.900	0.10	0.210	0.120	2.00	2.30	0.50	3.10	0.275	0.10	US

## PicoGate Logic footprints

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## REVISION HISTORY

Rev	Date	Description
_2	20021029	Second version (9397 750 10634). Supersedes AN10161_1 of 30 August 2002 (9397 750 10267).
_1	20020830	Initial version (9397 750 10267).

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