AN10365

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Application note

Surface mount reflow soldering

Abstract: This application note provides guidelines for the board mounting and handling of Nexperia surface mount packages.

Keywords: surface mount, reflow soldering, component handling, inspection, repair

nexperia

1. Introduction

This application note provides guidelines for board mounting of surface mount semiconductor packages. Reflow soldering is a widely spread technology for soldering of surface mount semiconductor packages. For many semiconductor packages, such leadless packages, reflow soldering is the only suitable method.

This application note describes the materials for reflow soldering: the Printed-Circuit Board (PCB), semiconductor packages and solder paste. One of the key features of the PCB is the footprint design. The footprint design describes the recommended solder land on the PCB to make a reliable solder joint between the semiconductor package and the PCB. A proven solder material is Sn/Ag/Cu (SAC). Process requirements for solder paste printing, component placement, and reflow soldering are also discussed in this application note. This document concludes with sections on inspection, repair and component handling.

2. Materials

2.1. Printed-circuit boards and footprints

Printed-Circuit Boards (PCBs) are not only used as mechanical carriers for electronic components, they also provide the electronic interconnection between these components and between these components and the outside world. These electronic components may be semiconductors, or other types such as capacitors and resistors. Through component selection and the use of Cu interconnections between the components, an electronic system, such as a mobile phone, can be assembled on a PCB. The substrates used for mounting the packages can be made of a variety of materials with different properties such as FR4, FR5, BT, flexible polymers (polyimide or polyamide) etc.

Due to the increased transistor density in the latest semiconductor technologies, and higher current (power) handling requirements, generation of heat has become a major limitation of semiconductor performance. By applying an exposed pad or heat sink in the semiconductor package, in combination with thermal vias in the PCB, the heat can be transferred from the active die to the outside world. In case of via in pad, the via should be capped and plated. The surface should be flat to avoid disruption to the soldering process. Optionally, thermal vias can be filled by copper or conductive epoxy.

Common solder land finishes include NiAu, Organic Solderability Preservative (OSP), and immersion Sn. Although finishes may look different after reflowing, and some appear to have better wetting characteristics than others, all common finishes can be used, if they are in accordance with the specifications.

Examples of other issues in board quality are tolerances on the pad and solder resist dimensions, maximum board dimensions, and flatness.

The application board is usually a mix of large and small components together with thermal design features. In board designs where large components or thermal design features are near small components, assembly issues may arise.

A footprint design describes the recommended dimensions of the solder lands on the PCB and the required stencil openings and thickness to make reliable solder joints between the semiconductor package and the PCB. The package outline and PCB footprints of Nexperia packages can be found by visiting the Nexperia package portal: https://www.nexperia.com/support/packages.html

For general guidelines on board design, see IPC-7351: Generic requirements for surface mount devices and land pattern standard.

The next paragraph explains how to read the PCB footprint. Fig. 1 shows an example of a PCB footprint, as found on the Nexperia web site.

Footprint information for reflow soldering of TSSOP16 package **SOT403-1**

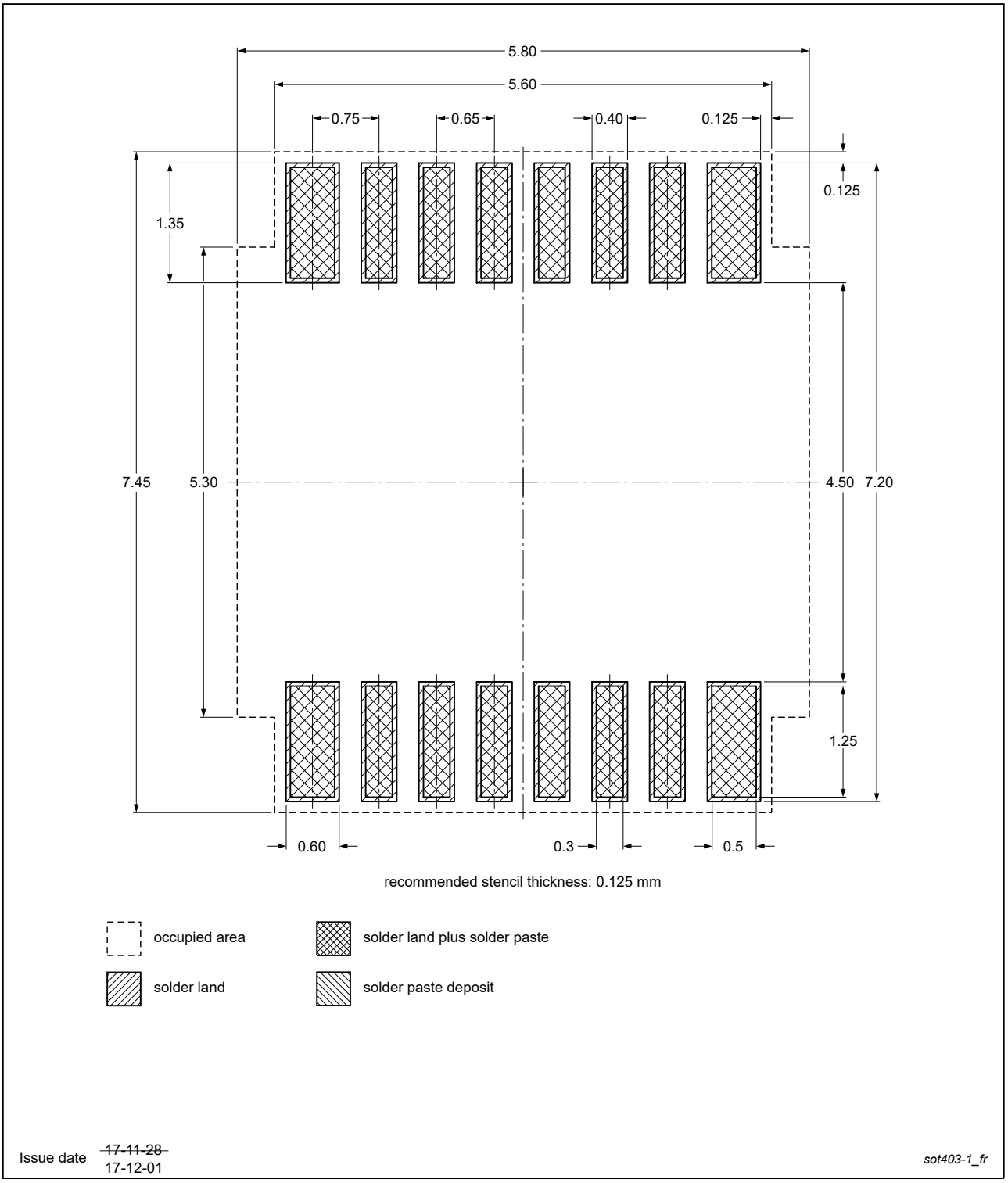

Fig. 1. PCB footprint and stencil dimensions for the SOT403-1 package (TSSOP16)

The soldering process is carried out under a set of process parameters that include accuracies in the process, such as component and solder paste placement accuracy, the board, the stencil and the semiconductor package itself. The footprint design is directly related to these aspects of the soldering process. The calculation of these dimensions is based on process parameters that are compliant with modern machines and a state-of-the-art process.

A solder resist layer (also known as a solder mask layer) is usually applied to the board to isolate the solder lands and tracks. If this solder resist extends onto the Cu, the remaining area to be soldered is solder resist defined. This area is sometimes referred to as Solder Mask Defined (SMD). Fig. 2 shows solder resist defined pads; yellow is Cu and dark green is solder resist. The Cu underneath the solder resist is shown in a lighter shade of green.

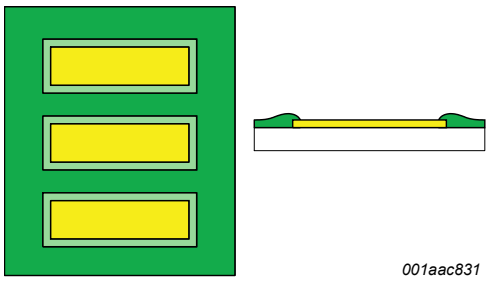

Fig. 2. Solder resist defined solder lands

The alternative situation is that the solder resist layer starts outside of the Cu. In that case, the solder lands are Cu defined. This situation is sometimes referred to as Non-Solder Mask Defined (NSMD). A Cu defined layout is shown in Fig. 3 (white is the bare board).

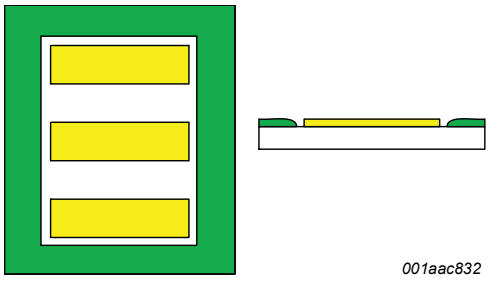

Fig. 3. Cu defined solder lands

A layout can also be partially solder resist defined and partially Cu defined.

Note that a solder resist defined layout requires the application of a solder resist bridge between two terminals. There is a minimum width of solder resist that can be applied by board suppliers. This fact, in combination with a maximum solder resist placement accuracy, implies that solder resist defined layouts are not always possible. For semiconductor packages with a small pitch, it is not possible to apply a solder resist bridge between two terminals. Either a Cu defined or combination layout, must be used.

If a solder land is solder resist defined, the Cu must extend far enough underneath the solder resist to allow for tolerances in Cu etching and solder resist placement during board production. Similarly, if a solder land is Cu defined, the solder resist must lie sufficiently far away from the solder land to prevent bleeding of the solder resist onto the Cu pad. Typical values for these distances are 25-50 µm.

The footprints referred to in this document indicate the areas that can be soldered.

The footprint shown in Fig. 2 is redefined for both a solder resist and a Cu layout in Fig. 4. Note that the overlap/gap between the solder resist and the Cu is 0.05 mm in this example.

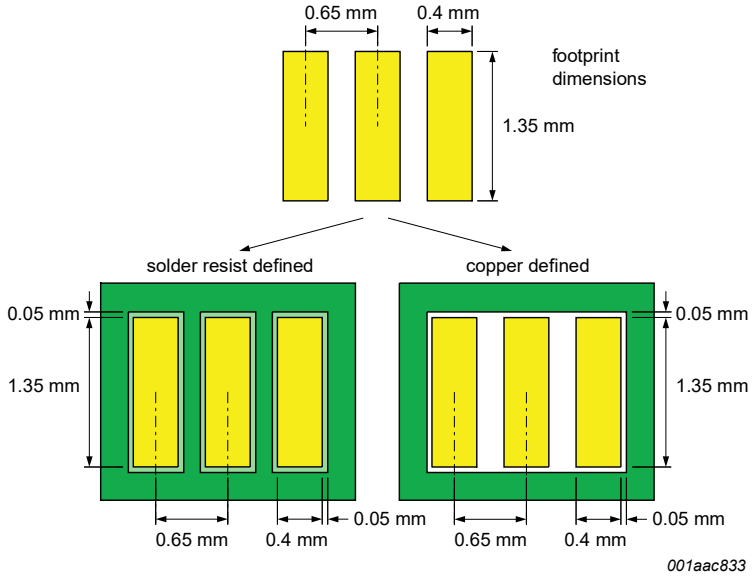

Fig. 4. Solder land dimensions for SOT402 package, either solder resist or Cu defined

Section 10 shows MicroPak (near Chips Scale Package Land Grid Array type package) soldering information on WLCSP/BGA footprint.

2.2. Semiconductor packages

Semiconductor surface mount packages can be divided into groups. In this document, they are categorized according to the shape of the terminals, as this has the largest influence on board assembly. The three main semiconductor family types are:

- leaded packages
- leadless packages with solder lands
- leadless packages with solder balls

Apart from the terminals, packages can have heat sinks and/or ground connections.

A lot of Nexperia packages have galvanic Sn plating finish on the leads to guarantee a good wettability at soldering. These are the measures to suppress the growth of Sn whiskers for automotive qualified products (refer to quality standard as on product page):

- Matte Sn is used for plating
- The plating thickness is minimum 7 µm (following JP002)
- There is a baking step (1 hour, 150 °C) after Sn plating

Alternative lead finishes are:

- NiPdAu plating
- E-less Sn plating
- Solder balls

Leaded packages

- Coplanarity of the leads is an important issue. To prevent the occurrence of open circuits or bad joints, coplanarity must be within the specifications (refer to the package outline drawing). Poor coplanarity may also increase problems caused by board warpage.
- Where the tips of leads are cut out of the lead frame, they do not need to be wetted after reflow.
- Leaded packages can be reflow soldered. Standard gullwing packages can only be wave soldered if the lead pitch is equal to, or larger than, 0.65 mm and no exposed heatsink is present. Wave soldering smaller pitches leads to a higher defect level.

a. Gullwing b. Flatpack

Fig. 5. Example of leaded packages

Leadless packages with solder lands

- The exposed lead frame edges at the sides of the semiconductor packages are often not finished, these do not have to be wetted for a proper joint. Leadless packages with side wettable flanks need to be wetted by solder.
- Possible solder land finishes are NiPdAu or Sn.
- Leadless packages with solder lands can only be reflow soldered, they cannot be wave soldered.

Fig. 6. Example of leadless packages with solder lands

In a standard DFN/QFN/SON package, the sides of the terminals consist of bare Cu. As a result, the sides of the terminals may not be wetted during reflow soldering. Non-wetting failures are difficult to detect in DFN/QFN/SON packages.

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Fig. 7. QFN/SON package with 'wettable flank'

A 'wettable flank' option may be requested for variants of these packages with a terminal pitch ≥ 0.5 mm. Non-wetting of the sides can be detected more easily with the wettable-flank option, simplifying the inspection process.

Fig. 8. Example of ultra-small leadless DFN packages with solder lands

The main advantage of small leadless packages is that they need very little board space for a given function of a semiconductor device. These packages, however, are more susceptible to mechanical damage due to their size and construction than standard gullwing packages or packages with relatively large soldering areas. Excessive sheer forces acting on the side of the body of the device or excessive bending of the board can easily cause the device to be damaged or dislodged. Compliance with international board mounting standard IPC-A-610 is recommended when working with boards.

During manual processes such as physical inspection, the moving of boards to other locations and/or other manual handling processes, there is risk of damage to ultra-small leadless packages.

Special care is needed if flexible substrates (e.g., thickness in the range 0.1 mm - 0.2 mm) are used. They are designed to be folded, but excessive bending, at positions where semiconductor packages are placed, must be excluded. During transportation in production, supporting with carrier tools (frames) is highly recommended.

The risk of damage is greater if the devices are mounted near the edge of the board rather than towards the center of the board. In the center, small components can be surrounded by other components, that provide a form of protection.

Manual touching should be avoided. If manual handling is unavoidable, handle with care and avoid applying shear forces of more than 4 N to the sides of the devices. An assembled board should be held by the edges (see Fig. 9) or handled while contained in a specially designed cassette or another dedicated carrier tool (frame).

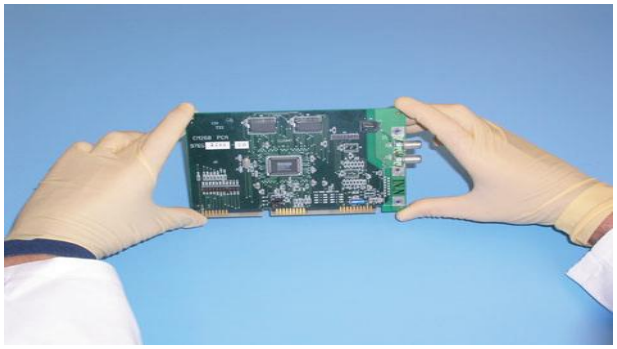

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Fig. 9. Manual handling of an assembled board

Semiconductor packages can have heat sinks at the top or the bottom of the package. The following remarks apply to packages with heat sinks at the bottom, such as DHXQFNs:

- Even if it is not required to solder the exposed pad to the board for electrical or thermal purposes, the package reliability may improve if it is.
- Voids in the solder joint connecting the heat sink pad to the board are allowed, if it does not conflict with demands made by the application.

Fig. 10. Thermally enhanced leadless packages with solder lands

Leadless packages with solder balls

- These semiconductor packages are particularly good at self-alignment, as the package body is suspended over molten solder during reflow. This practice results in a package type with a robust reflow soldering process.
- The balls are made of SAC solder.
- Packages with solder balls can only be reflow soldered and not wave soldered.

Fig. 11. Leadles package with solder balls

For (FO)WLCSP there is a dedicated application note (AN10439).

2.3. Solder paste

In line with European legislation, it is recommended to use Pb-free solder paste, although exemptions are granted for selected applications, such as automotive.

A wide variety of Pb-free solder pastes are available, containing combinations of tin, copper, antimony, silver, bismuth, indium, and other elements. The different types of Pb-free solder pastes have a wide range of melting temperatures. Solders with a high melting point may be more suitable for the automotive industry. Solders with a low melting point can be used for soldering consumer semiconductor packages.

The most common Pb-free paste is SAC, which is a combination of tin (Sn), silver (Ag), and copper (Cu). Alloys contain usually 3 % to 4 % Ag and 0 % to 1 % Cu, which is near eutectic. SAC typically has a melting temperature of around 217 °C, and it requires a reflow temperature of minimum 235 °C.

A no-clean solder paste does not require cleaning after reflow soldering and is therefore preferred, if it is possible within the process window. If a no-clean paste is used, flux residues may be visible on the board after reflowing. For packages with low stand-off height such as MicroPak, cleaning underneath the package is difficult; therefore, a no-clean paste is recommended.

Use solder particles type 3, type 4 or type 5, for best print definition. Storage and use conditions as specified by the solder paste supplier should be followed. A solder ball test can be used to verify the reflow properties of the solder paste (IPC-TM-650, Solder Ball Test). Before using the paste, it should be allowed to reach room temperature in the closed pot and next be thoroughly mixed.

For more information on the solder paste, contact your solder paste supplier.

3. Moisture sensitivity level and storage

If there is moisture trapped inside a package, and the package is exposed to a reflow temperature profile, the moisture may turn into steam, which expands rapidly. This expansion may damage the inside of the package (delamination) and result in a cracked semiconductor package body (the popcorn effect). The sensitivity of a package to moisture is the Moisture Sensitivity Level (MSL). It depends on the package characteristics and the temperature it is exposed to during reflow soldering.

The MSL of semiconductor packages can be determined through standardized tests in which the packages are moisturized to a predetermined level and then exposed to a standardized temperature-time profile. Studies have shown that small and thin packages reach higher temperatures during reflow than larger packages. Therefore, small, and thin packages must be classified at higher reflow temperatures, see Table 1.

Table 1. Pb-free process - Package classification reflow temperatures (from J-STD-020)

Package thickness	Volume ($<350\ mm^3$)	Volume ($350\ mm^3$ to $2000\ mm^3$)	Volume ($>2000\ mm^3$)
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm to 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

The temperatures that packages are exposed to during MSL determination are always measured at the top of the package body.

Depending on the damage after this test, an MSL of 1 (not sensitive to moisture) to 6 (very sensitive to moisture) is attached to the semiconductor package. For every product, this MSL is given on a packing label on the shipping box. Each package is rated at two temperatures, for SnPb and Pb-free soldering conditions. An example of a packing label is given in Fig. 12

Fig. 12. Example of MSL information on packing label; note the two MSLs corresponding to the two reflow processes

An MSL corresponds to a certain out-of-bag time (or floor life). If semiconductor packages are removed from their sealed dry-bags and not soldered within their out-of-bag time, they must be baked prior to reflow. Baking removes any moisture that might have soaked into the package. MSLs and temperatures on the packing labels are to be always respected. Naturally, this also means that semiconductor packages with a critical MSL may not remain on the placement machine between assembly runs. Nor should partly assembled boards, between two reflow steps, be stored longer than indicated by the MSL level.

The semiconductor package floor life, as a function of the MSL, can be found in Table 2.

Table 2. Floor life as a function of MSL

Refer to IEC 61760-2 Transportation and storage conditions of surface mounting devices and/or IPC/JEDEC J-STD-033B.1 Handling, packing, shipping and use of moisture/reflow sensitive surface mount devices.

MSL	Floor life	
	Time	Conditions
1	unlimited	≤ 30 °C/85 % RH
2	1 year	≤ 30 °C/60 % RH
2a	4 weeks	≤ 30 °C/60 % RH
3	168 hours	≤ 30 °C/60 % RH
4	72 hours	≤ 30 °C/60 % RH
5	48 hours	≤ 30 °C/60 % RH
5a	24 hours	≤ 30 °C/60 % RH
6	6 hours	≤ 30 °C/60 % RH

4. Surface mounting process

4.1. Solder paste printing

Solder paste printing requires a stencil aperture to be completely filled with paste. When the board is released from the stencil, the solder paste adheres to the board and all the paste is released from the stencil aperture. This ensures that a good solder paste deposit remains on the board. Ideally, the volume of solder paste on the board should equal the 'volume' of the stencil aperture.

The filling of the stencil openings depends mainly on the squeegee speed and pressure, the squeegee material, the size of the solder particles in the solder paste and on the solder paste rheology. A soft squeegee can scoop out the paste in the stencil openings. To avoid this a big stencil opening can be divided into multiple smaller openings. However, the recommended option is to use a metal squeegee.

The release of the paste out of the stencil opening depends mainly on the stencil opening dimensions and stencil thickness. If a stencil opening becomes very small, the paste no longer releases completely. Furthermore, stencil apertures must be larger if a thicker stencil is used. Also, the shape of the stencil opening plays a role. The opening should be at least equal size or slightly larger at the bottom. The side walls should be smooth.

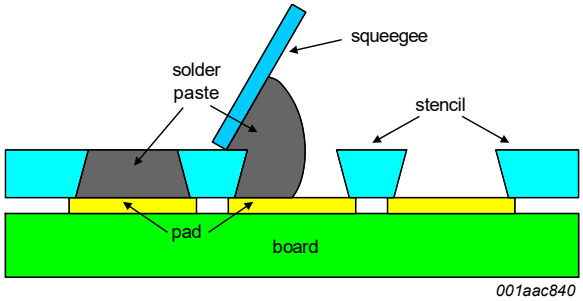


Fig. 13. Stencil printing

Guideline for stencil opening dimensions:

- Top (print) side: design value +0/-20 µm
- PCB side: design value ±12 µm

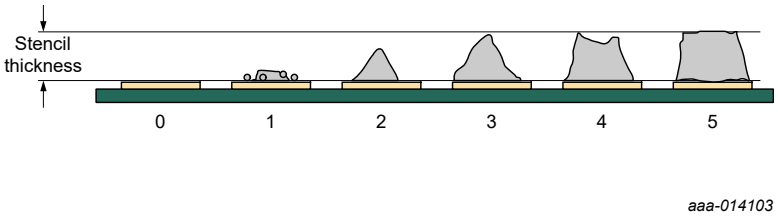
Stencils are commonly made from Nickel. An electroformed or laser cut stencil is recommended. An electroformed stencil has the most accurate openings. Typical stencil thicknesses are given in Table 3

Table 3. Typical stencil thickness

Package pitch (mm)	**Stencil thickness (µm)**
0.65	100-125
0.4 or 0.5	100
0.35 or 0.4	80-100
0.3	60
Package size (metric)	**Stencil thickness (µm)**
1005	100-125
0603	75-100
0402	50-80

To achieve a difference in solder paste volumes on one board, it is possible to use a stencil that has a different thickness at different locations: a step-stencil. However, the step-stencil is only recommended if there is no other solution. With a step-stencil only rubber squeegees can be used since metal squeegees cannot go into the step area.

During stencil printing the print speed and pressure should be adjusted such that the stencil is wiped clean of paste and the solder paste rolls in front of the squeegee nicely. In essence, all parameters must be adjusted so that all solder paste deposits on one board, from the smallest to the largest, are printed properly. If needed, the bottom side of the stencil can be cleaned regularly to avoid smearing. Criteria for print definition and smearing are given in Fig. 14 and Fig. 15.



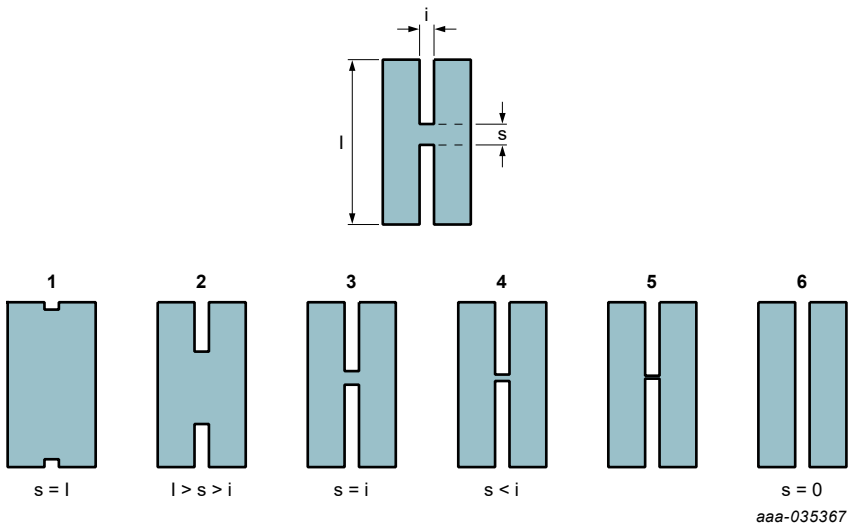
0) No solder paste
1) Irregular shape (few balls)
2) Pyramid, lower than stencil thickness
3) Pyramid, height equal to stencil thickness
4) Beginning flat-top with “dog ears”
5) Flat-top side

3, 4 and 5 are acceptable rankings.

Fig. 14. Ranking for definition of solder paste deposits

The consequences of insufficient solder paste printing are usually open contacts or bad joints. Possible causes are:

- The solder paste deposit is not sufficiently high and components or their leads may not make proper contact with the paste, resulting in open circuits or bad joints,
- There is insufficient solder volume for a proper solder joint, resulting in open circuits,
- The activator is used up rapidly in a small solder paste deposit, so that the paste no longer properly wets the component metallization, resulting in open circuits.



5 and 6 are acceptable rankings.

Fig. 15. Ranking for smearing of solder paste deposits

Smearing arises as follows: If some solder paste bleeds between the stencil and the board during one printing stroke, the next board may not fit tightly to the stencil. A loose fit allows more paste to bleed onto the bottom of the stencil. Once this effect starts, it strengthens itself. As a result, the solder paste may eventually form bridges that stretch from one paste deposit to the next. If a bridge is narrow enough, it snaps open during reflow, as the volume of molten solder seeks to attain minimum surface area. A wider bridge, however, may remain stable, resulting in a short-circuit. The degree of smearing depends on the gap between the stencil and the PCB (snap-off distance), the

solder paste type, the frequency of bottom side stencil cleaning, the distance between the stencil openings and the solder land definition on the PCB. SMD solder lands are more prone to smearing.

A general rule is that the stencil apertures must be 25 µm smaller than the solder lands, on all sides. In other words, the solder paste lies 25 µm inward from the solder land edge. This results in stencil aperture dimensions that are 50 µm smaller than the corresponding solder land dimensions; see Fig. 16. By exception, sometimes 50 µm or 0 µm reduction on all sides is being used.

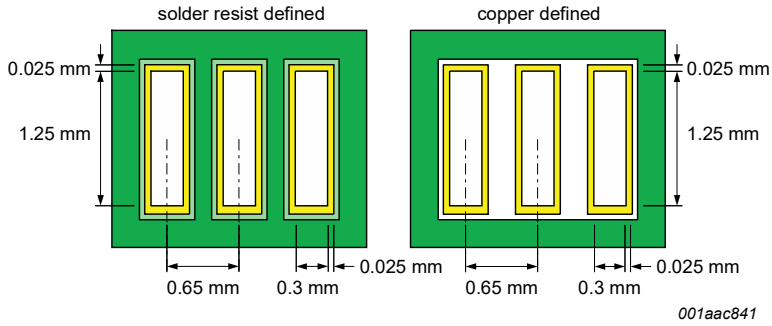


Fig. 16. Solder paste printing on copper and solder resist defined solder lands

An exception lies with the very large solder lands, such as when printing solder paste on a heatsink land. In that case, print an array of smaller solder paste deposits. The solder paste should cover approximately 30-65 % of the total land area. It is also advisable to keep the solder paste away from the edges of this land. The solder paste pattern, including the spacing between the deposits, should have a coverage of 50-85 % of the land area (see Fig. 17 and Fig. 18). The reason for this is that the flux in solder paste on the heat sink pads starts boiling (already before the solder melts). The gas finds a way out towards the IO pads taking liquid flux and solder paste or melted solder with it causing solder balls, solder bridges and open solder joints. By reducing the solder paste volume on the heat sink pad and keeping the solder paste away from the edge of the heat sink pad, the risk of defects is lowered.

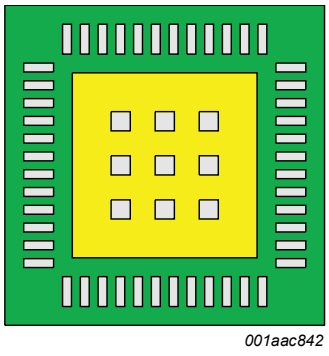


Fig. 17. Paste coverage

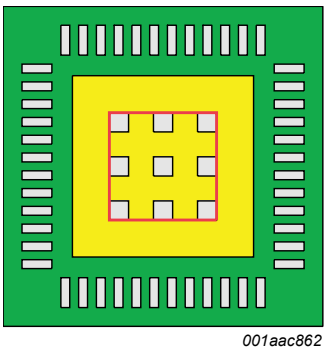


Fig. 18. Pattern coverage

A paste printing pattern for exposed die pads is illustrated by the example shown in Fig. 19. An HWQFN24 with an exposed pad of 2.45 mm × 2.45 mm, for example, should have nine solder paste deposits that are arranged in a three-by-three array. The solder paste deposits are 0.9 mm × 0.9 mm, and the distance between them is 0.3 mm.

This way, the solder paste area is 4 × (0.9 mm × 0.9 mm). Dividing this by the land area 2.45 mm × 2.45 mm, yields a solder paste coverage of approximately 54 %.

Similarly, the solder paste pattern (the paste, plus the area between the deposits) has a length of 2.1 mm. The pattern area, 2.1 mm × 2.1 mm, divided by the land area, yields a paste pattern coverage of approximately 73 %.

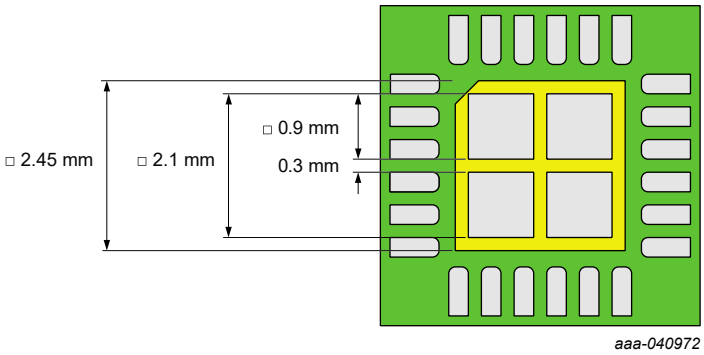


Fig. 19. Solder paste dimensions on the land area for an exposed die pad of HWQFN24

Depending on the solder paste used, the solder paste deposits printed on a large land may not always coalesce completely. In some cases, individual solder joints can still be recognized between the exposed die pad and solder land on the board. It is possible that voids remain in the solder joints. Whether or not voids or incomplete coalescing of the solder are a problem, depends on the application. For low-power devices in which little heat is generated, up to 80 % of voids may still be acceptable.

Keep in mind that printing a smaller volume of solder paste could have adverse effects on the solder joint reliability. Also, if there are vias in pads, solder paste deposits should be arranged so that paste is never printed directly over an open via.

4.2. Semiconductor package placement

The required placement accuracy of a package depends on various factors, such as package size, the terminal pitch, and the package type itself. During reflow, when the solder is molten, a package that has not been placed perfectly may center itself on the pads. This action is referred to as self-alignment. Therefore, if the package is a trusted self-aligner, the required placement accuracy of a package may be less tight.

Typical placement tolerances, as a function of the semiconductor package terminal pitch, are given in Table 4.

Table 4. Typical placement accuracy

Package terminal pitch	Placement tolerance (±3 sigma)
≥ 0.65 mm	100 µm
< 0.65 mm and > 0.5 mm	50 µm
< 0.5 mm	30 µm

Semiconductor packages are usually placed with two types of machines. If the highest placement accuracy is required, the slower but more accurate machines must be used. These machines are also often more flexible when it comes to unusual package shapes, that may require dedicated nozzles and non-standard trays. If the highest placement accuracy is not necessary, and there are no special requirements, fast component mounters or chip shooters, can be used. These machines can process up to 100,000 components per hour.

The placement force may also be an important parameter for some packages. In theory, a semiconductor package is always pressed down into the solder paste until it rests on a single layer of solder paste powder particles. Excess solder paste is pressed aside. A consequence is that the solder paste that is pushed aside, or that bulges outside the package, may cause bridges with neighboring solder paste deposits.

In extreme cases, solder paste may not only bulge outside the pads, but it may be blasted farther away from the pads. It results in a small amount of solder paste no longer being connected to the paste deposit from where it originally came. This effect must always be avoided as the splattered solder paste may cause a short circuit on the board. The original solder paste deposit may then have insufficient solder. This effect is often caused by using an improper nozzle shape, so that air from the nozzle blows the paste away.

If the placement force is too low, there is a chance that a semiconductor package terminal does not make sufficient contact with the solder paste. In that case, there is a risk that the solder paste tackiness is not able to hold it in place up to the reflow zone in the oven and the package may be displaced. In addition, even if the semiconductor package remains in place, there may be bad contact between the package terminals and the solder paste resulting in open contacts or bad joints.

The placement force must be adjusted so that there is no excessive paste bulging or splattering. There must be proper contact between the semiconductor package and the solder paste. The placement force necessary to achieve this contact, depends on several factors, including the package dimensions. Typical forces are 1.5 N to 4 N. Some of the more modern machines have a sensor that detects the proximity of the package to the solder paste. The proximity detection reduces the placement speed as soon as the package comes near to, or touches, the solder paste. In this way, splattering can be minimized. During component placement good board support is essential to enable the right placement force and to ensure a flat board during placement.

4.3. Reflow soldering

The most important step in reflow soldering is the reflow itself when the solder paste deposits melt, wetting takes place and solder joints are formed. This is achieved by passing the boards through an oven and exposing them to a temperature profile that varies in time.

A temperature-time profile essentially consists of four zones:

1. Heating zone, fast heating to reach a certain minimum temperature across the whole board.
2. Equalization zone, to equalize the temperatures across the board up to a certain temperature range to avoid larger temperature differences in the reflow zone. The length and temperature depend on the component mix on the board.
3. Reflow zone: the board is heated to a peak temperature that is well above the melting point of the solder but below the temperature at which the components and boards are damaged.
4. Cooling zone: the board is cooled down rapidly so that soldered joints freeze before the board exits the oven.

Before adjusting the reflow profile for a certain board, the locations of the spots with the lowest and highest temperatures need to be defined. Cold spots are usually found in sections of the board that hold a high density of large, thick components, as these soak up a lot of heat. Large areas of Cu in a board also reduce the local temperature. Hot spots are found in areas with few components, or only the smallest, thin components like discrete passives, and with little Cu. Finally, the board dimensions, and the board orientation in the oven, may also affect the location of hot and cold spots. A method to define the locations of the hottest and coldest spots is to dispense solder paste dots on a fully populated board, mainly on the solder joints, and run it through an oven with a relatively low temperature. The solder paste dot that melts first, is the hottest spot. After that, the reflow temperature is increased in steps until the last solder paste dot melts. This is the location of the coldest spot. After attaching thermo-couples to the hottest spots and coldest spots, usually solder joints, the reflow profile can be adjusted.

The reflow profile starts with a fast-heating zone from room temperature until the hottest spot on the board reaches a certain minimum temperature. Typically, this is 160-180 °C.

In the equalization zone the temperature of the hottest spot is kept more or less constant while the coldest spot is being heated as close as possible to the temperature of the hottest spot. The equalization zone should be kept as short as possible to avoid deterioration of the solder paste: the activator might run out. Please follow advice from you solder paste supplier.

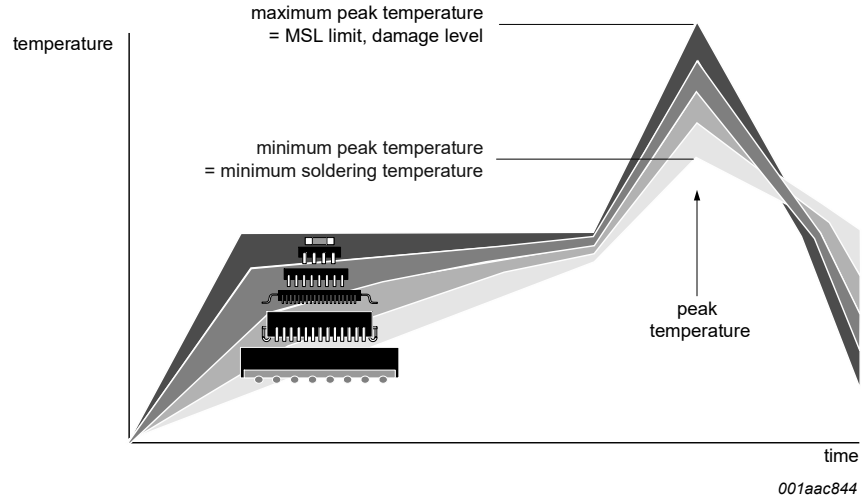


Fig. 20. Temperature profiles for large and small components

In Fig. 20, the light grey band with the large component represents the coldest spot, and the dark grey band, at the top, with the smallest component, represents the hottest spot..

The third phase in the reflow profile is the reflow zone, in which the solder melts and solder joints are formed. The peak temperature of the coldest spot should be the minimum temperature needed by the solder paste for good wetting and form reliable solder joints. A typical minimum temperature for SAC solder is 235 °C and for SnPb it is 215 °C. The coldest spot should always be measured in a solder joint because the requirement is based on the type of solder.

The temperature of the hottest spot should be such that the board including organic preservation finish and the components are not damaged. Please remind that the component top side is typically warmer than the solder joint. The thicker the package the greater the difference. E.g. for SO packages the difference is about 10 °C. Convection reflow ovens result in smaller temperature differences compared to IR reflow ovens.

Since the minimum temperature for SAC solder is higher than for SnPb solder while the maximum temperature is the same, the process window for SAC soldering is smaller, thus requiring tighter process control.

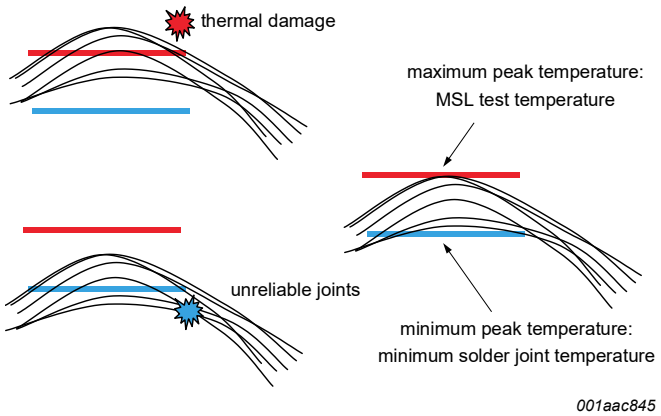


Fig. 21. Fitting both the hot and cold spots into the required peak temperature range

The black lines in Fig. 21 represent the actual reflow zones for several different temperature spots on a board. The bottom black line represents the coldest spot, and the top black line represents the hottest spot. The blue line represents the minimum peak temperature, and the red line is the maximum peak temperature. At the top left, some regions on the board are exposed to temperatures that are too high, exceeding damage limits. At the bottom left, some regions on the board are exposed to temperatures that are too low, resulting in unreliable joints. At the right, all the regions on the board have peak temperatures that fall within the upper and lower limits.

Reflow may be done either in air or in nitrogen. In most cases, nitrogen should not be necessary; in that case, air is preferred because of the lower cost. In general, a nitrogen atmosphere gives better wetting and better solder balling behavior of the solder paste. Reflow may be done in convection reflow ovens. Furthermore, using vapor phase reflow soldering can reduce temperature differences on a board. More info regarding the reflow profile can be found in Fig. 22 and Table 5.

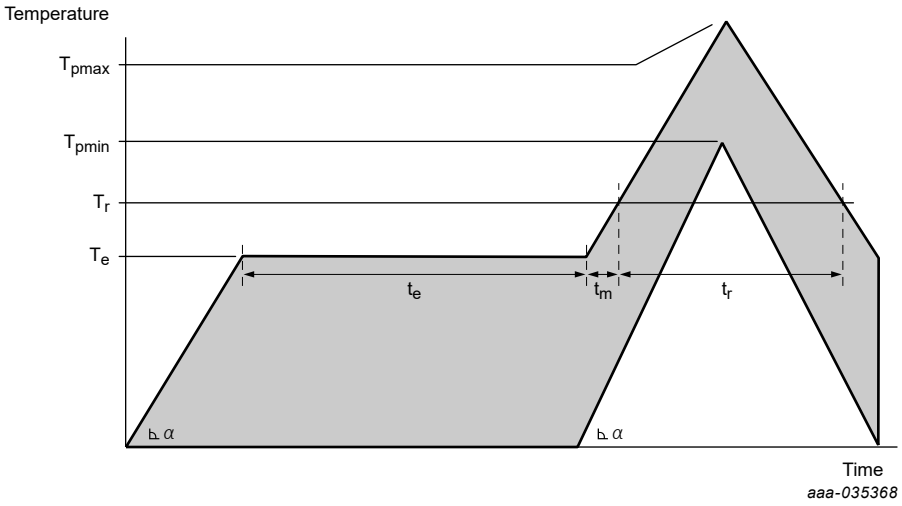


Fig. 22. Reflow profile requirements for SAC reflow soldering

Table 5. Explanation of the reflow temperature profile

Parameter	Value(s)	Remark
α	<10 °C/s	Please check solder paste and component (e.g. ceramic capacitors) and board limitations
T_e	160 °C to 180 °C	Below the liquidus temperature of the solder alloy
T_r	217 °C	Liquidus temperature (solder alloy dependent)
t_e	As short as possible, < 60 s preferred	Depends on the solder paste used - contact your solder paste supplier – solder balling and hot slump behavior might be affected. Hot slump might be avoided by pre-drying 45 min 45 °C.
t_r	< 70 s	Time above liquidus of the solder, with time the number of voids in the solder increases, weakening the solder joints
t_m	2-30 s	As short as possible, taking heating rate into account
$T_{p(min)}$	235 °C	Temperature measured in the solder at the coldest spot, depends on the solder alloy type
$T_{p(max)}$	260 °C	Depends on the board and the board finish (OSP is most critical) and the most temperature-sensitive component used on the board. $T_{p(max)}$ - $T_{p(min)}$ should be as small as possible.
Reflow atmosphere	-	General purpose reflow is under air atmosphere, nitrogen reflow is allowed

Application boards are usually populated with components on both sides of the board. This means that the board needs to undergo a soldering process twice. It is important, therefore, that the following details are considered prior to a double-sided reflow process to prevent damage to, or malfunction of the components.

- Components should be able to withstand multiple reflow cycles. As components are MSL classified, they are guaranteed to withstand three reflow cycles.
- If the time between first and second reflow exceeds the floor life of the corresponding MSL classification, the application board must be dried before the second reflow. Storage between reflow steps in a nitrogen cabinet or sealed MBB is also an option.

- Heavy components mounted during the first reflow may drop off during the second reflow, either due to their weight or because of vibration during transport through the reflow oven. Heavy components may be fixed in place with glue.
- The first reflow step might deteriorate the wettability of the solder land finish on the second reflow side, especially OSP is very critical. The maximum.. reflow temperature for the first reflow step might have to be lowered. Soldering in nitrogen will also help.

4.4. Solder and terminal finish or solder ball compatibility

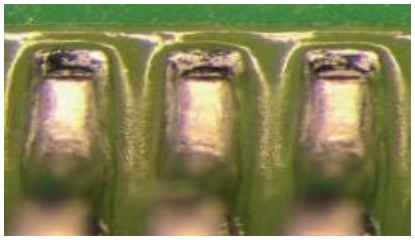
When selecting a solder paste, care must be taken that the solder is compatible with both the board and the semiconductor package finishes. When soldering leaded or leadless packages, Pb-free package finishes can be combined freely with all solders.

It is not recommended to combine SAC solder balls with SnPb solder paste. During the reflow the solder balls will not melt which might affect the solder joint reliability.

5. Inspection and repair

5.1. Inspection

In general, Pb-free solder is a little less successful at wetting than SnPb solders. SAC fillets have a larger contact angle between the fillet and the wetted surface. When using Pb-free solder, the contact angle is typically 20° to 30°. Notice the difference between SnPb and Pb-free solder in Fig. 23. The photograph on the left (SnPb) shows that the solder lands have been completely wetted. The photograph on the right shows that the solder has left part of the solder lands unwetted.



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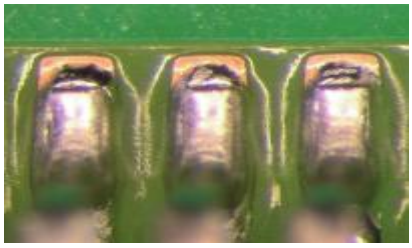
a. SnPb solder joints

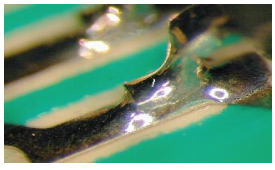


001aac863

b. Pb-free solder joints

Fig. 23. Difference in wetting between SnPb and Pb-free solder joints

Another visual aspect in Pb-free soldering is that Pb-free solder joints tend to be less shiny than SnPb solder joints and they may have striation marks. This is due to the different microstructure that is formed during solidification. Although SnPb solder joints should be rejected if they look this way, it is normal for Pb-free and no reason to reject Pb-free solder joints.



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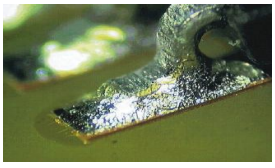
a. SnPb solder joints



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b. Pb-free solder joints

Fig. 24. Difference in appearance between SnPb and Pb-free solder joints

Non-wetting of lead frame parts as a result of punching or sawing is not a reason for rejection.

Other inspection methods besides optical inspection, such as, for design and process development purposes are:

- Automatic optical inspection (AOI)
- Examination by röntgen ray (X-ray)
- Cross-sectional analysis
- Dye penetration test

5.2. Repair

Sometimes, a package lead that has not been soldered properly may be repaired simply by heating this single lead with the tip of a soldering iron. In this case, it is sufficient to heat the lead until the solder melts completely; a new device should not be necessary.

In other situations, there may be a need to replace a semiconductor package on the board. In that case, the rework process should comprise the following steps:

1. Device removal
2. Site preparation
3. Application of solder paste to the site
4. Device placement
5. Device attachment

Dry bake the board for 4 hours at 125 °C prior to steps 1 to 5. If needed the new device should also be dry baked. This will depend on the MSL level and the time out of bag. The repair steps are summarized in Fig. 25.

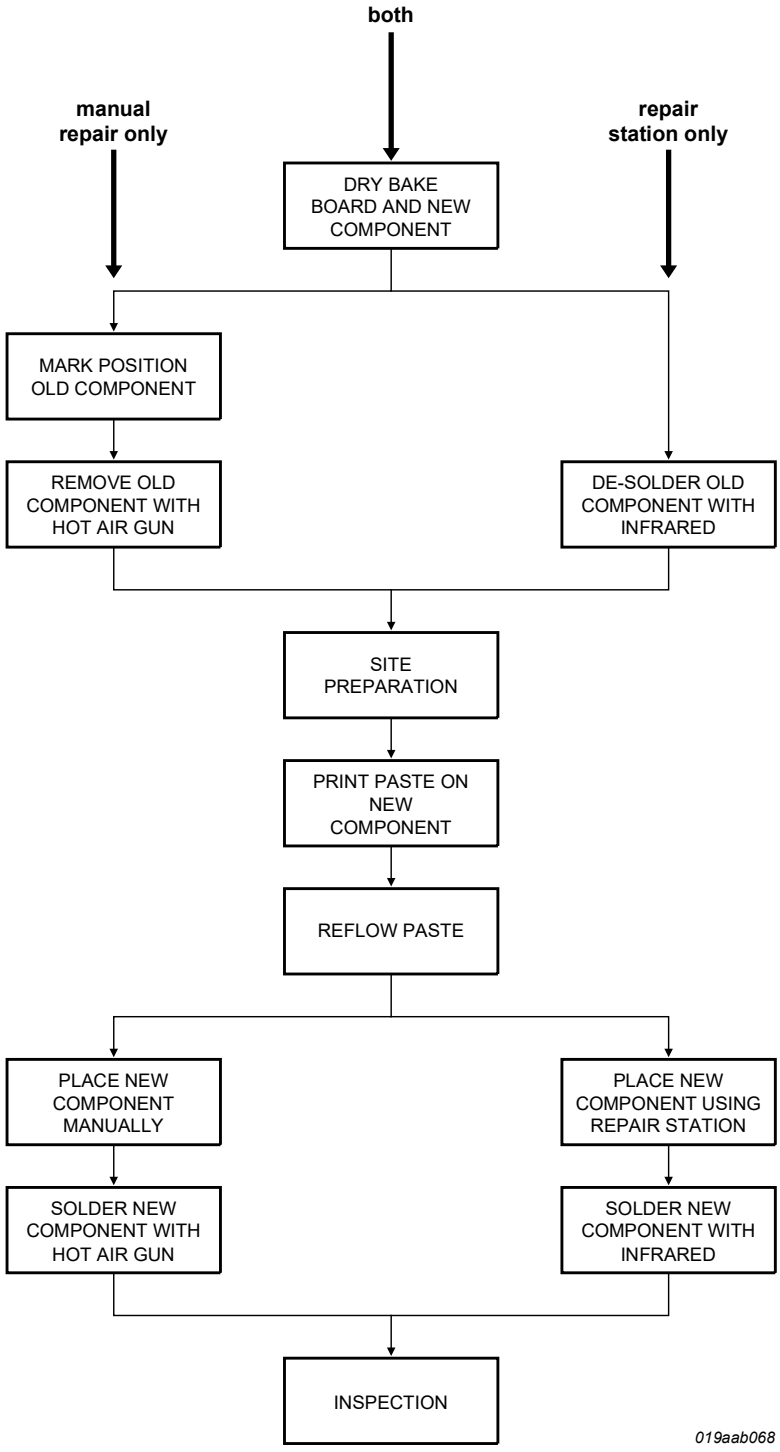

Fig. 25. Rework process steps

5.2.1. Device removal

In order to remove a semiconductor package from the board, it must be heated. If possible, the heating must be done as locally as possible to avoid heating the surrounding board and components. Packages with leads at a relatively large pitch may first be removed from the board by cutting the leads, after which only the leads must be de-soldered. De-soldering can be done with a soldering iron.

Semiconductor packages without leads must be heated entirely for removal. Heat can be supplied using a hot air gun, a soldering iron, or focused infrared energy, depending on the package type and availability. If necessary, the bottom of the board can also be heated. The temperature to which the package solder joints should be heated depends on the solder that was originally used. It is best to keep the temperature as low as possible, just above the melting point of the solder alloy used.

As soon as the solder has melted, the semiconductor package is lifted from the board using a vacuum wand or tweezers. Note that package removal should not be initiated until the solder has melted entirely.

Reuse of removed semiconductor packages is not recommended.

5.2.2. Site preparation

After the device has been removed, the board area must be prepared for the new device. Prepare the site by removing any excess solder and/or flux remains from the board. Ideally it can be done on an appropriate de-soldering station, using solder wick or an alternative method.

After most of the solder has been removed from a solder land, a very thin layer of solder will be left on top of a few intermetallic layers. In the case of Cu boards for example, there are layers of Cu_3Sn, Cu_6Sn_5 and finally solder, on top of the Cu. The top layer of solder is easily soldered.

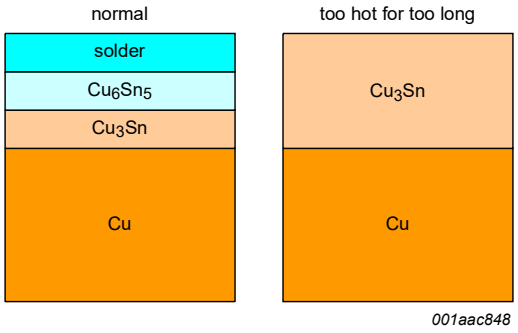

Fig. 26. Overheating and Cu_3Sn formation

If, however, the pad is heated too much during removal of the rejected semiconductor package and during site preparation, the top two layers are also converted into Cu_3Sn. In this case, there is only the Cu_3Sn intermetallic layer on top of the Cu. Unfortunately, Cu_3Sn is hardly wettable, as a result, it becomes very difficult to solder the replacement package at this location. Therefore, care must be taken during reject package removal and site redress that the solder lands are heated not more than necessary.

5.2.3. Solder paste printing

After the site redress is completed, solder paste should be applied to either the site or the device. This can be done by using a miniature stencil or other in-house techniques. Preferably, the same type of solder paste should be used as was originally applied on the board.

If the new device that is to be soldered to the board has solder balls, solder paste printing is not necessary. In this case, it suffices to apply a thin layer of tacky flux on the solder lands on the PCB.

5.2.4. Device placement

The last step of the repair process is to solder the new semiconductor package on the board. If necessary, the new package may be aligned under a microscope or split beam system, possibly in a special repair station. If this is not possible, try to align the device with board markers.

5.2.5. Soldering

To reflow the solder, apply a temperature profile that is as close as possible to the original reflow profile used for assembling the board. Take care that the board and/or semiconductor package are not moved or tilted until the solder has solidified completely. Note that if a board is exposed to reflow temperatures a second time, it may be necessary to dry bake the board for the sake of the components that have already been mounted.

6. Component handling

6.1. Electrostatic charges

Damage to semiconductors from ElectroStatic Discharge (ESD) is a major cause of rejects and poses an increased risk to miniaturized packages. Electrostatic charge can be stored in many things, for example, man-made fiber clothing, moving machinery and objects with air blowing across them. It can also be stored in plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people. Electrostatic discharge is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. It is recommended that the following ESD precautions are complied with.

6.1.1. Workstations for handling ESD sensitive components

Fig. 27 shows a working area suitable for safely handling electrostatic-sensitive devices. The following precautions should be observed.

- Workbench and floor surface should be lined with anti-static material
- Persons at a workbench should be earthed via a wrist strap and a resistor
- All mains-powered equipment should be connected to the mains via an earth leakage switch
- Equipment cases should be grounded
- Relative humidity should be maintained between 40 % and 50 %
- An ionizer should be used to neutralize objects with immobile static charges in case other solutions fail
- Keep static materials, such as plastic envelopes and plastic trays away from the workbench. If there are any such static materials on the workbench remove them before handling the semiconductor devices.
- Refer to the current version of the handbook EN 100015 (CECC 00015) "Protection of Electrostatic Sensitive Devices", which explains in more detail how to arrange an ESD protective area for handling ESD sensitive devices

6.1.2. Receipt and storage of components

Packing for electrostatic devices should be made of anti-static/conductive materials. Warning labels on both primary and secondary packing show that the contents are sensitive to electrostatic discharge. The electronic components should be kept in their original packing while in storage. If a bulk container is partially unpacked, the unpacking should be done at a protected workstation. Any electronic components that are stored temporarily should be repacked in conductive or anti-static packing or carriers.

6.1.3. PCB assembly

All tools used during assembly, including soldering tools and solder baths, must be grounded. All hand tools should be of conductive or anti-static material and where possible should not be insulated. Consider the standard precautions for manual handling of electrostatic-sensitive devices.

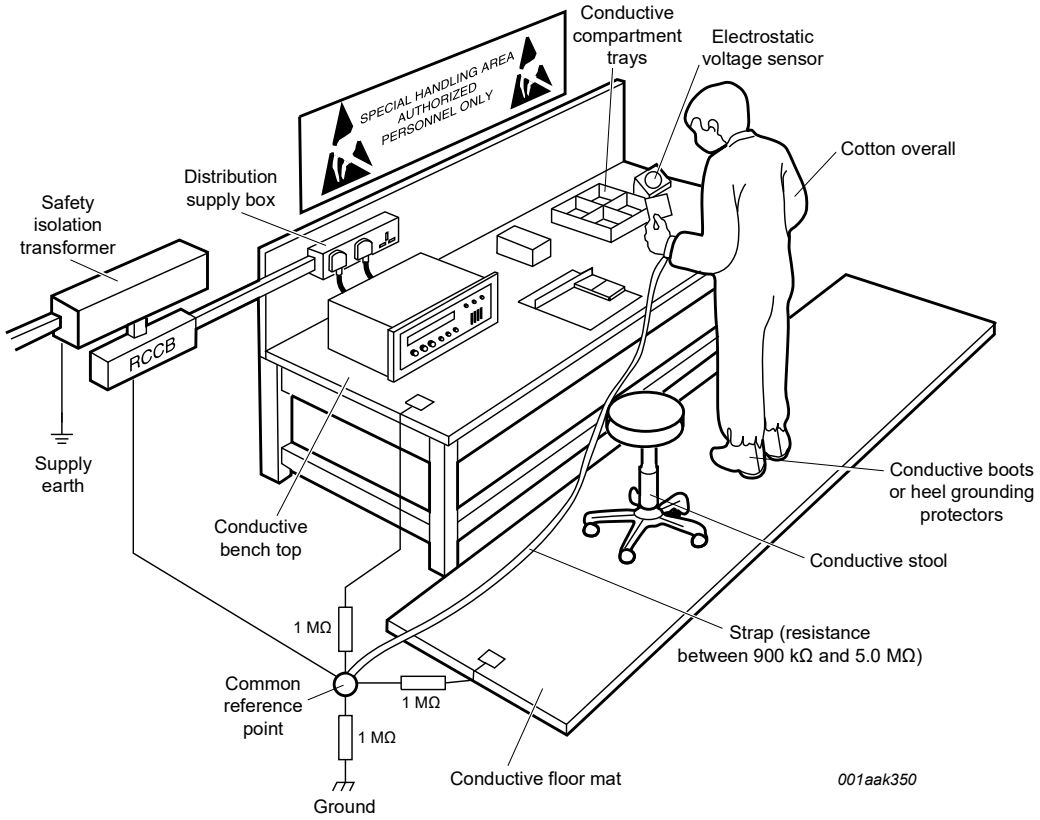

Fig. 27. ESD protected workstation environment

7. Abbreviations

Table 6. Abbreviations

Acronym	Description
AOI	Automatic Optical Inspection
BT	Bismaleimide Triazine
DFN	Dual Flat No Leads
ESD	ElectroStatic Discharge
FR	Flame Resistant
FOWLCSP	FanOut Wafer-Level Chip-Scale Package
HVQFN	Heatsink Very thin Quad Flat-pack No leads
MBB	Moisture Barrier Bag
MSL	Moisture Sensitivity Level
NMSD	Non Solder Mask Defined
OSP	Organic Solderability Preservative
PCB	Printed Circuit Board
QFN	Quad Flat-pack No leads
QFP	Quad Flat Package
RCCB	Residual Current Circuit Breaker
SAC	Solder Alloy Consisting of tin, silver and copper
SMD	Solder Mask Defined
SON	Small Outline No leads
TSSOP	Thin Shrink Small Outline Package
WLCSP	Wafer-Level Chip-Scale Package
URL	Uniform Resource Locator

8. Revision history

Table 7. Revision history

Rev	Date	Description
AN10365 v.9	20250326	• Section 2.2 updated
AN10365 v.8	20240905	• Section 2.1: Reference added to appendix A • Section 4.1: Solder coverage and dimensions changed. • Fig. 19 added.
AN10365 v.7	20220902	• The text and format of this application note has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.
AN10365 v.6	20120730	• Amendments to Section 2.4
AN10365 v.5	20110906	• Added Section 2.4
AN10365 v.4	20090813	• Text amendments to Section 2.1, 2.3, 4.3, 5.1; Section 6 “Component handling” added; items added to Section 8 “References”; Export control disclaimer added to Section 9.2 “Disclaimers”.
AN10365 v.3	20080422	• Various text amendments to Section 1, 2.1, 2.2, 2.3, 3, 4.1, 4.2, 4.3 and 6.

Rev	Date	Description
AN10365 v.2	20060726	• Updates in Table 1, Table 8 and on page 20: the minimum peak reflow temperature when using SnPb solder is changed from 210 °C to 215 °C.
AN10365 v.1	20050524	• Initial version.

9. References

[1] IPC/JEDEC J-STD-020D August 2007: Joint Industry Standard Moisture/Reflow, Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[2] IEC 61760-2: Transportation and storage conditions of surface mounting devices

[3] IPC-7351: Generic requirements for Surface Mount Design and Land Pattern Standard, IPC

[4] EN 100015/CECC 00015: Protection of Electrostatic Sensitive Devices, European Standard

[5] IPC-A-610H: Acceptability of Electronic Assemblies, IPC

[6] AN10439: (Fanout)Wafer level chip scale package

[7] IPC-TM-650: Test Methods Manual

10. Appendix A: MicroPak soldering information for WLCSP/BGA footprint

The MicroPak package is a near Chips Scale Package (CSP) Land Grid Array (LGA) type plastic encapsulated package with a copper lead frame base.

Fig. 28 shows the recommended solder land pattern for mounting the MicroPak XSON6 (SOT886) package. Using this pattern results in a very good electrical and mechanical connection which can also be inspected and tested for continuity.

Although the footprint for the Texas Instruments WLCSP/BGA package is physically smaller, the MicroPak very easily fits the same footprint. Fig. 29 shows the recommended solder land pattern for the WLCSP/BGA package and the footprint of the MicroPak SOT886.

Placing the WLCSP/BGA package on the MicroPak footprint is not recommended. As can be seen in Fig. 30 the larger land pattern for the MicroPak may cause solder starvation due to the limited amount of solder in the package solder ball. Solder paste would help, although there will be limited mechanical contact. This is true for the larger Pb-free WLCSP/BGA balls. Even less mechanical contact is achieved with the smaller PbSn WLCSP/BGA balls.

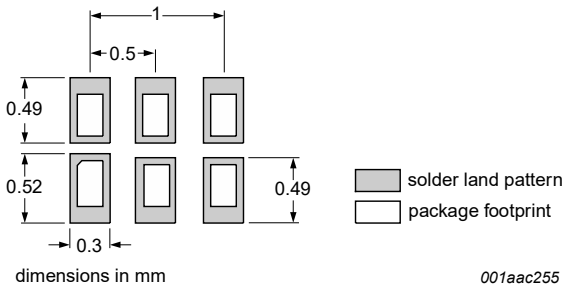

Fig. 28. MicroPack footprint

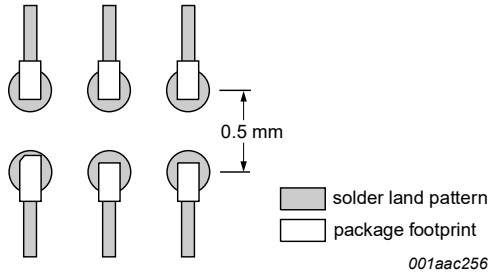

Fig. 29. MicroPack SOT886 on BGA footprint

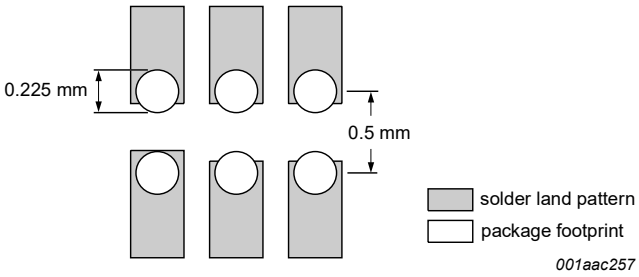

Fig. 30. BGA on MicroPack footprint

11. Legal information

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Date of release: 26 March 2025