AN90032

Low temperature soldering, application study

Rev. 1.1 — 22 February 2022 application note

Document information

Information	Content
Keywords	Low Temperature Soldering, LTS, SnBiX, board mounting, SMT, reflow
Abstract	This application note investigates SMT assembly using Low Temperature Solder (SnBiX) in reflow lines for Nexperia packages. Board mounting, thermal and mechanical behavior are analyzed. All Nexperia packages can be soldered using SnBiX solder pastes.

1. Introduction

New generation Low Temperature Solder (LTS) pastes for Surface Mount Technology (SMT) is proposed for low temperature applications such as computing. LTS pastes are commonly build on near-eutectic SnBi alloying system and therefore show reduced melting temperatures which reduces the reflow temperatures as well as the energy consumption during SMT by up to 40%. This translates into reduced CO_2 emissions and reduced manufacturing cost. Additionally, such effect can improve the yield impact created by high temperature (HT) warpage. HT warpage is widely recognized seen as main driver to reduce the reflow temperature for SMT. New product markets such as ultra-mobile computing and the Internet of Things (IoT) drive the need for smaller and thinner packages and boards which can suffer warpage by reflow temperatures of current solder systems like SAC. By lowering the peak temperature during reflow, warpage is reduced, resulting in higher SMT yields.

To safeguard the usage of Nexperia products on LTS assembly lines an internal investigation was carried out proving LTS readiness of Nexperia's package families. This application note will give details on the analysis and guideline for possible use of LTS solder.

Since Nexperia's package portfolio consists of various lead finish technologies, family representatives of these technologies were selected and mounted on a printed-circuit board (PCB) using standard SAC and new LTS solder.

2. LTS application study

To safeguard potential application of Nexperia products in LTS assembly lines, a range of packages were validated compared to standard SAC solder. By that valuable insights of LTS assembly were gained and will be shared.

Six representative packages were subjected to the following test plan:

- 0 hour characterization:
  - Ceramic plate test
  - Microsection
  - Optical inspection
  - X-ray inspection
- Board level Reliability
  - Thermal cycling
  - Drop testing
- Mechanical testing
  - Shear testing

3. Set up and Materials

3.1. Package selection

Various packages have been chosen to cover Nexperia's plating and leadframe technologies. Fig. 1 shows the selection. Six products were used in this application study.

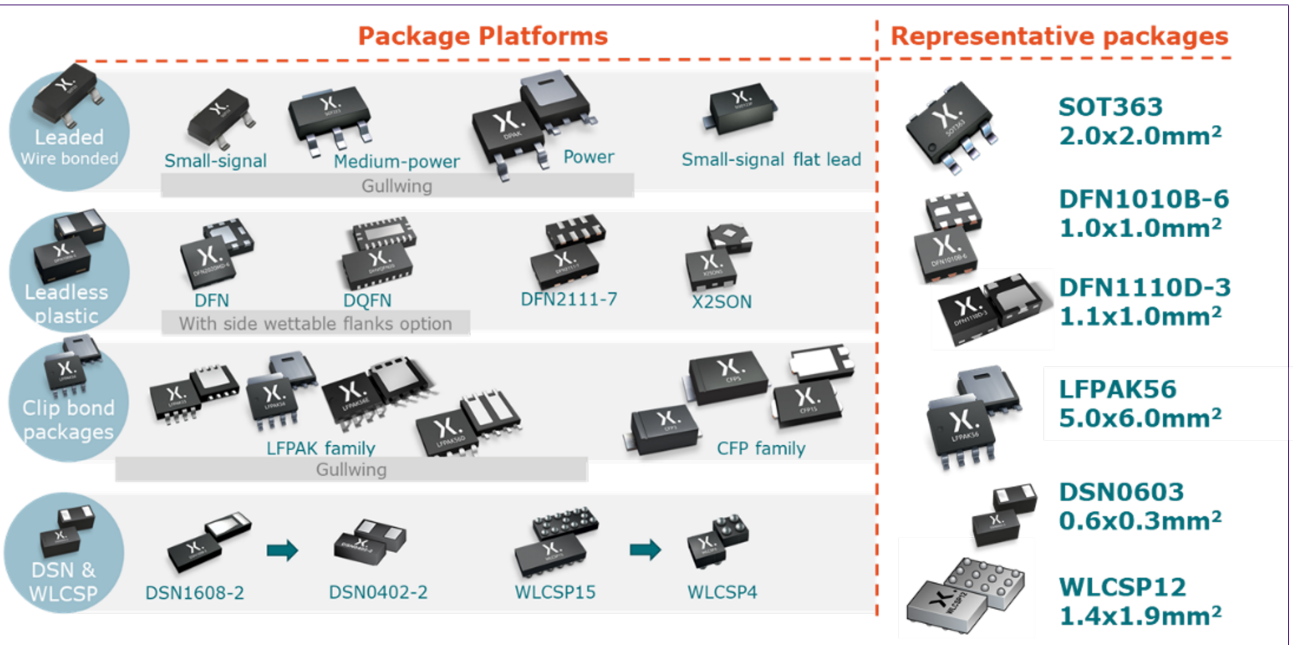


Fig. 1. Package selection

This selection covers:

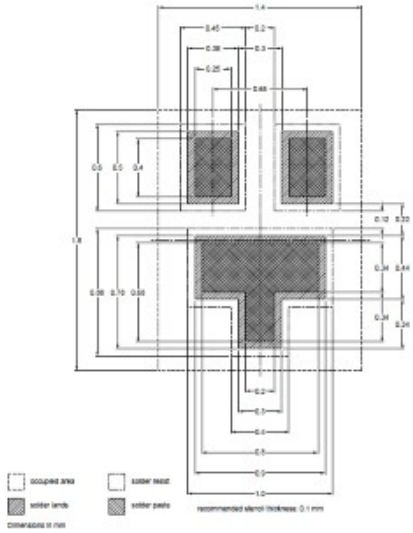
- SOT363: NiFe leadframe + Cu plating and Sn finish
- DFN1010B-6 (SOT1216), DFN1110D-3 (SOT8015) Cu leadframe with NiPdAu plating and Sn finish
- LFPAK56 (SOT669): Cu leadframe with Sn finish
- WLCSP12: WLCSP with SAC solder balls
- DSN0603-2 (SOD962): DSN with CuSn pads

3.2. Footprint and stencil design

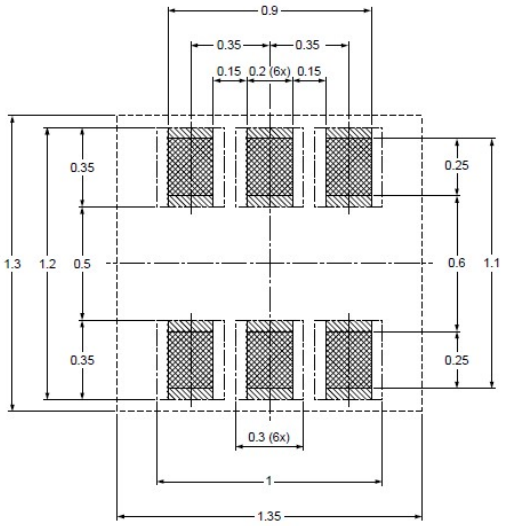
Footprint and stencil design were chosen according to product recommendations for the selected packages, see Fig. 1.

As PCB material, 8 layer FR4 boards according to JESD22-B111/A104 were used. WLCSP12 and DFN1110D-3 were assembled on drop test PCB layout while the other packages were soldered on reliability boards. The footprints used are shown in Fig. 2, (see also Appendix 1) and examples of PCBs in Fig. 3.

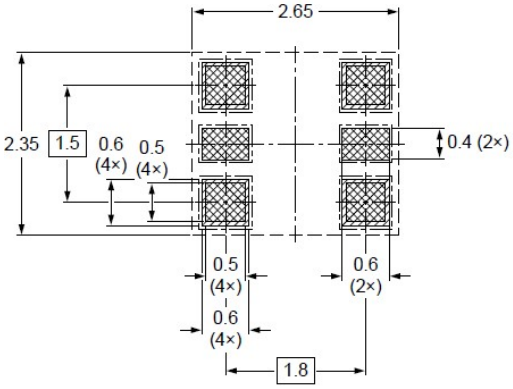
DFN1110D-3



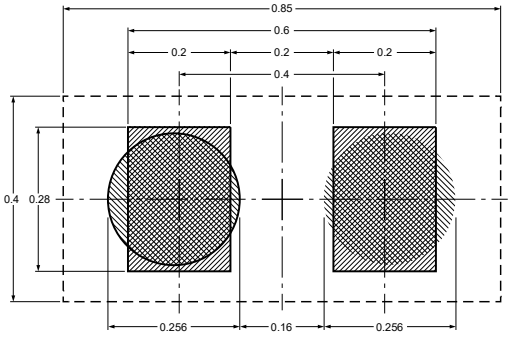
DFN1010B-6



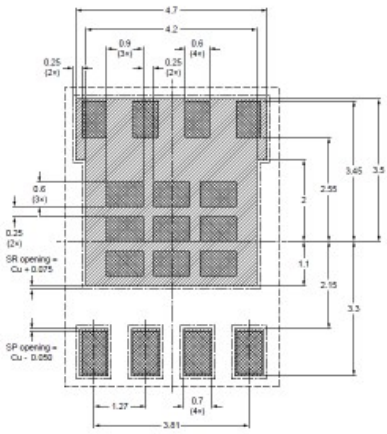
SOT363



DSN0603



LFPAK56



WLCSP12

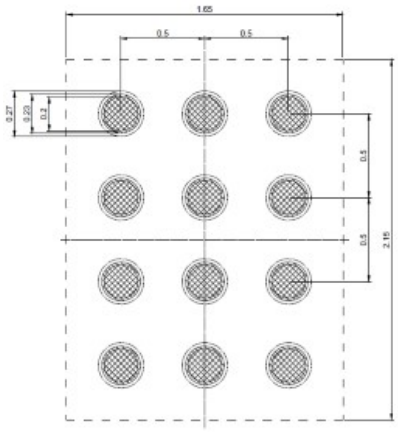
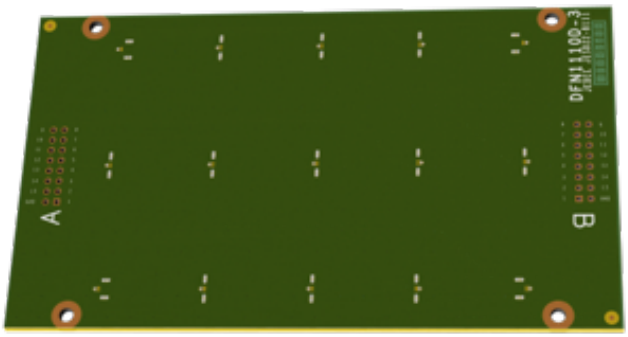
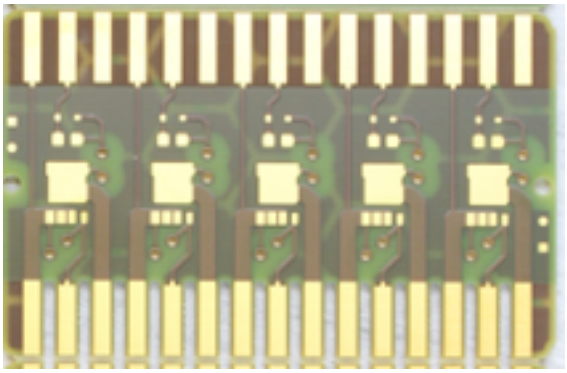


Fig. 2. Examples of footprints used



drop test PCB (DFN1110D-3)



reliability test PCB (LFPAK56)

Fig. 3. Examples of drop test PCB and reliability PCB

3.3. Solder paste

As Low Temperature Solder paste, a commercially available, near eutectic SnBiX alloy (Sn42Bi57.6Ag0.4) Type 5 was used. As comparison, trails were conducted using SAC305 Type 4.5 alloy. Further paste printing details are shown in Table 1.

Table 1. Solder paste printing details

Package	Stencil thickness [µm]	Print speed [mm/s]	Squeegee force [N]
DSN0603	80	40	45
DFN1010-6	100	35	49
DFN1110D-3	100	35	55
SOT363	100	35	49
LFPAK56	120	35	49
WLCSP12	80	40	45

4. Reflow profile

Reflow profile should be adjusted according to the data sheet of the solder material supplier. Soldering was done under nitrogen atmosphere.

Fig. 4 shows the profile of SnBiX solder compared to SAC solder used in the application study.

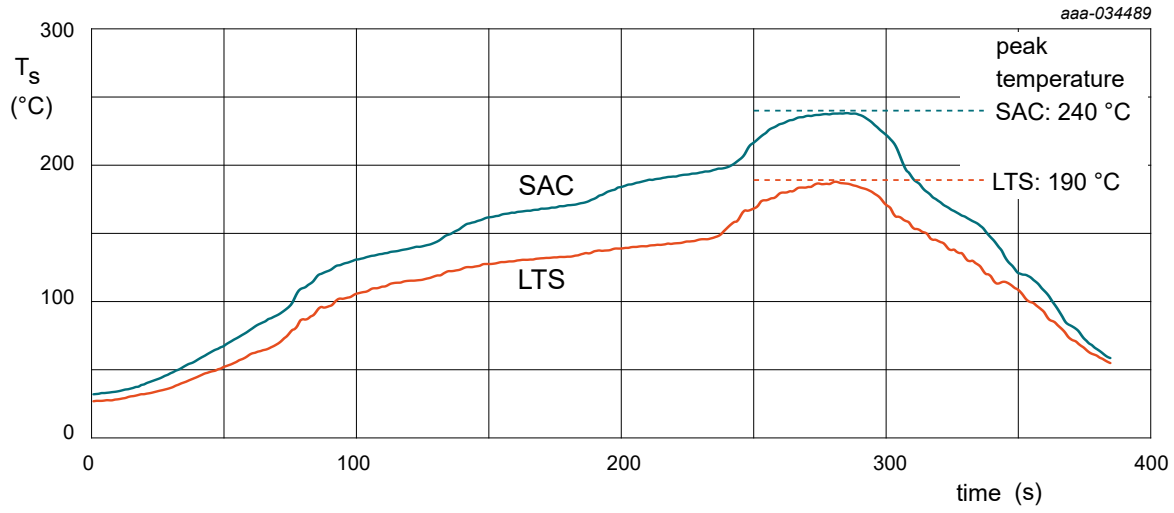


Fig. 4. Reflow profile for LTS and SAC solder pastes

5. Results

5.1. 0 hour characterization

5.1.1. Ceramic plate test

In the ceramic plate test, solder paste is printed onto a ceramic substrate, followed by package placement and reflow. Further, the reflowed solder on the leads of the package is visually inspected to determine the wetting characteristics.

- Wetting performance of all packages are according to requirements (>95%)
- No difference in wetting performance between LTS and SAC

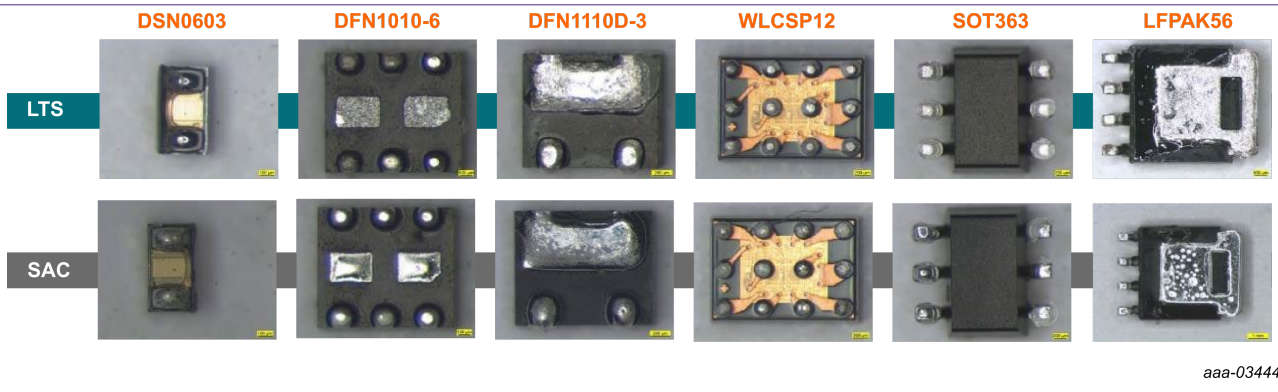


Fig. 5. Wetting performance

5.1.2. Optical inspection

No significant differences between LTS and SAC solder paste except for slightly higher solder paste volume when using LTS solder have been observed. Better release performance of LTS solder paste is suspected because of different flux system.

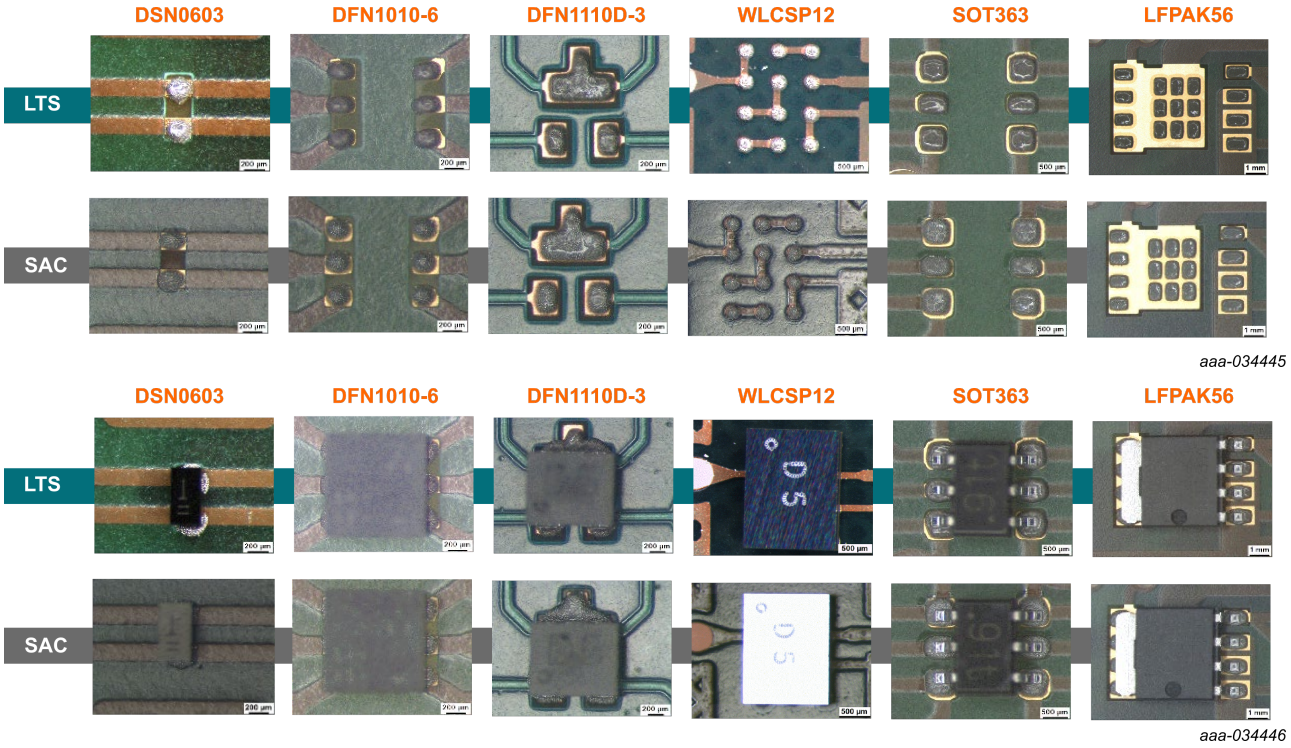


Fig. 6. PCB after solder paste printing and placement

5.1.3. Microsection

Microsection images of all packages confirms good wettability of LTS and SAC solder. Both alloys show homogeneous inter-metallic compounds (IMC). For SnBiX alloy, lamellar Bi-Sn microstructure is visible. WLCSP12 forms hybrid joint to SAC solder ball while the solder ball does not collapse during reflow.

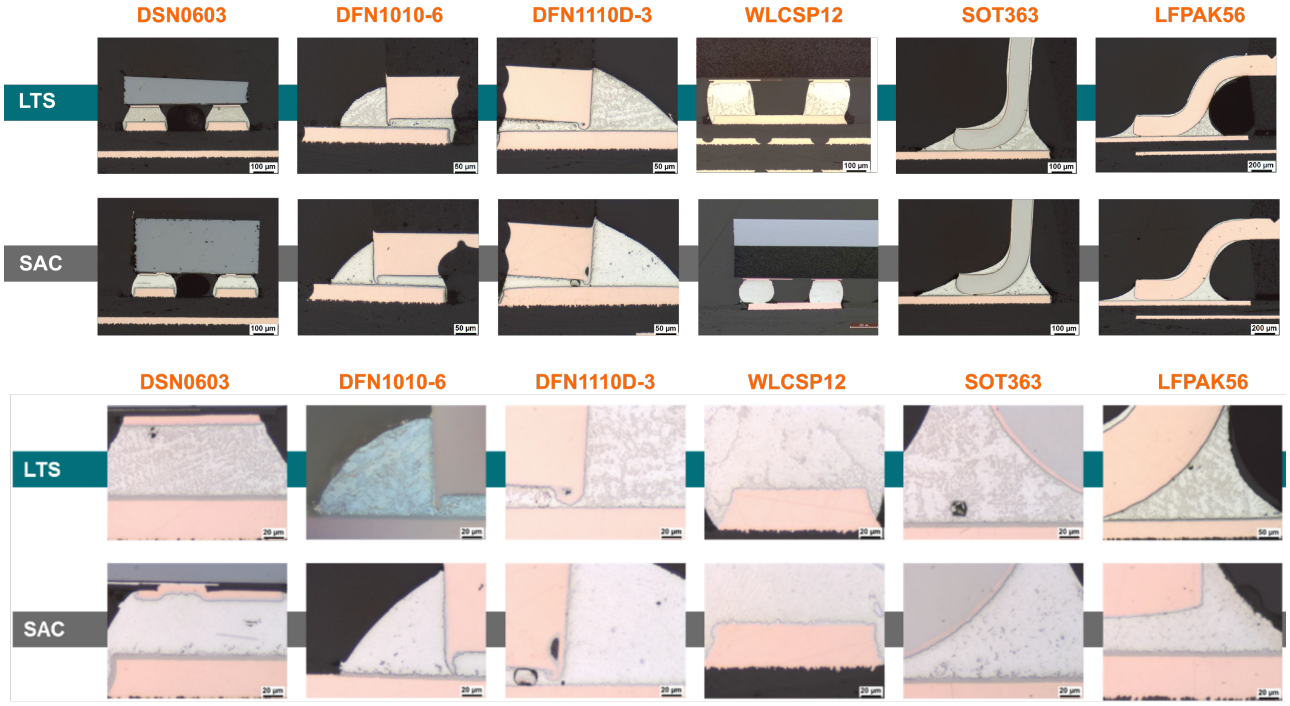


Fig. 7. Microsections of LTS and SAC solder joints after reflow

5.1.4. X-ray inspection

X-ray inspection to cross check the wetting performance and solder voids. No significant difference between LTS and SAC solder is visible in X-ray.

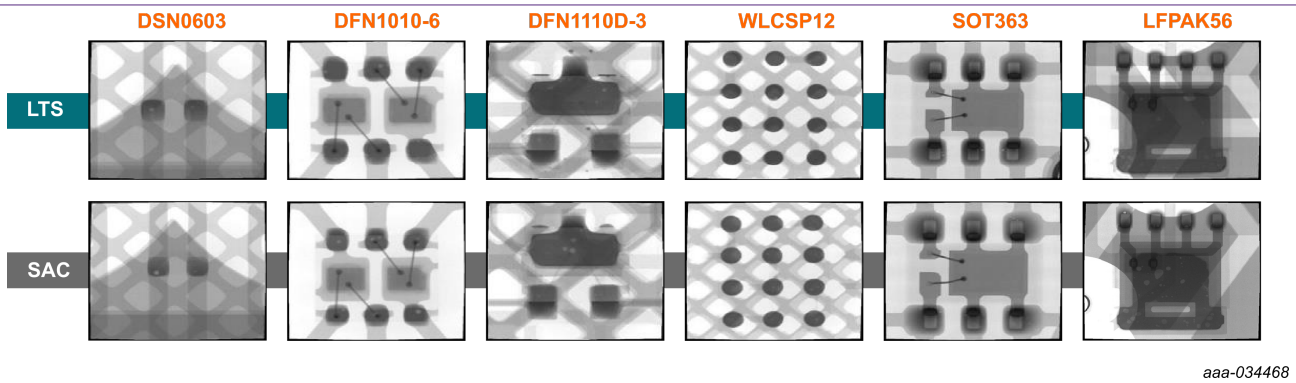


Fig. 8. X-ray inspection after reflow

5.2. Board level reliability

5.2.1. Thermal cycling

Temperature cycling test was executed (TCT / JESD22-A104D) according to condition N and G for LTS soldered samples, see Table 2. Electrical testing after soldering on PCB and after TCT was done with the standard tests per type. For DFN1110D-3 and WLCSP12 daisy chain samples with in-situ resistance monitoring in TCT were used.

No solder related differences could be detected between devices soldered with SAC and LTS. For LTS solder joints, grain coarsening was observed after 1500 cycles as shown in Fig. 9.

Table 2. TCT conditions according to JESD22-A104D

Test condition	Nominal $T_{s(min)}$ with tolerances	Nominal $T_{s(max)}$ with tolerances
A	-55 (+0,-10)	+85 (+10,-0)
B	-55 (+0,-10)	+125 (+15,-0)
C	-65 (+0,-10)	+150 (+15,-0)
G	-40 (+0,-10)	+125 (+15,-0)
H	-55 (+0,-10)	+150 (+15,-0)
I	-40 (+0,-10)	+155 (+15,-0)
J	-0 (+0,-10)	+100 (+15,-0)
K	-0 (+0,-10)	+125 (+15,-0)
L	-55 (+0,-10)	+110 (+15,-0)
M	-40 (+0,-10)	+150 (+10-0)
N	-40 (+0,-10)	+85 (+10,-0)

In addition to required testing condition N for computing applications, TCT condition G has also been passed on all tested products soldered with LTS. Samples soldered with SAC solder paste were tested as a direct reference.

Table 3. TCT results for condition N and G

Number of cycles	Number of failures / total											
	DSN0603-2		DFN1010B-6		SOT363		LFPAK56		DFN1110D-3		WLCSP12	
	LTS	SAC	LTS	SAC	LTS	SAC	LTS	SAC	LTS	SAC	LTS	SAC
0	0/80	0/80	0/75	0/80	0/80	0/80	0/80	0/80	0/60	0/60	0/48	0/48
500	0/80	0/80	0/75	0/80	0/80	0/80	0/80	0/80	0/60	0/60	0/48	0/48
750	0/80	0/80	0/75	0/80	0/80	0/80	0/80	0/80	0/60	0/60	0/48	0/48
1000	0/80	0/80	0/75	0/80	0/80	0/80	0/80	0/80	0/60	0/60	0/48	0/48
1250	0/80	0/80	0/75	0/80	0/80	0/80	0/80	0/80	0/60	0/60	0/48	0/48
1500	0/80	0/80	0/75	0/80	0/80	0/80	0/80	0/80	0/60	0/60	0/48	0/48

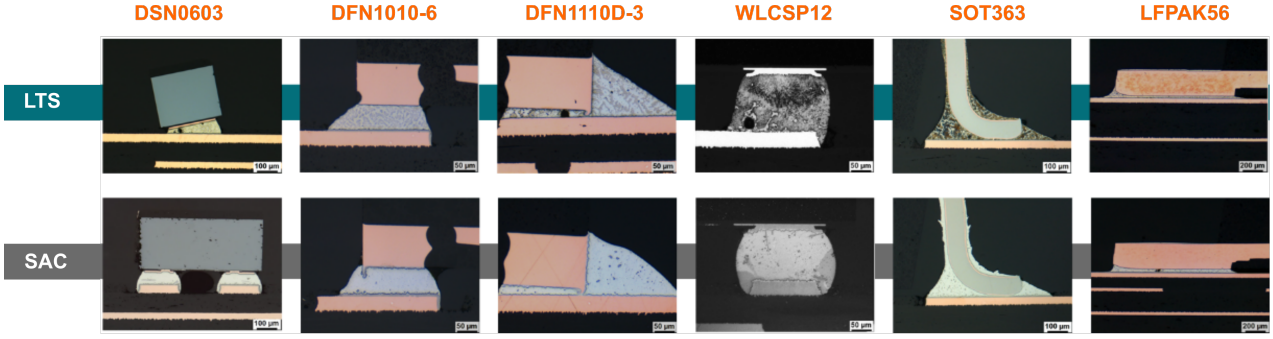


Fig. 9. Microsection after 1500 cycles, exemplary for condition N

5.2.2. Drop testing

Two packages were tested, WLCSP (hybrid solder joint) and DFN1110D-3. Both packages were tested according to JEDEC specification (JESD22-B111) and drop test was performed for samples soldered with SAC and LTS solder paste.

Both packages passed the JEDEC requirements (>100 drops) and withstood >2000 drops with no occurrence.

6. Mechanical testing

6.1. Shear testing

Package shear strength was determined at 0 hour condition and after 1500 cycles TCT (condition N). Shear strength at 0 hour is found slightly higher for LTS solder compared to SAC solder joints as expected from higher mechanical strength of LTS solder reported in data sheet. All solder joints show acceptable shear strength degradation after 1500 cycles, compare Table 4.

All packages fulfill industry established requirements.

Table 4. Shear testing results

Package	Shear strength [N]			
	0 cycles		1500 cycles	
	LTS	SAC	LTS	SAC
DSN0603	5.88 ± 0.20	5.49 ± 0.20	4.81 ± 0.29	4.90 ± 0.78
DFN1010-6	13.14 ± 0.69	12.26 ± 0.78	12.94 ± 1.57	11.08 ± 0.59
DFN1110D-3	28.64 ± 4.51	24.61 ± 3.43	27.36 ± 3.53	22.95 ± 2.16
WLCSP12	11.38 ± 0.69	12.26 ± 0.59	12.26 ± 0.20	11.77 ± 0.49
SOT363	17.46 ± 1.57	11.57 ± 0.20	14.51 ± 0.69	11.28 ± 0.10
LFPAK56	339.41 ± 32.56	265.56 ± 49.62	324.21 ± 33.24	278.12 ± 18.93

7. Conclusion

An extensive application study has been run on LTS assembly covering all Nexperias package platforms. Paste printing, wettability and product placement have shown comparable performance to SAC solder assembly.

After careful adjustment to LTS reflow profile, the reflow process can be run analogue to known procedures. LTS solder joints proved comparable performance, reliability has been proven by board level reliability (thermal cycling), drop test performance and joint strength in comparison to SAC solder joint.

Lower overall energy input and peak temperatures during reflow will reduce system warpage and energy consumption.

Thermal cycling was tested up to 125 °C (condition G), however customers are responsible in which application LTS will be applied.

All Nexperia packages can be soldered with no special precautions using SnBiX solder pastes.

8. Further remarks

Stencil design

For small solder pads an optimization of stencil apertures individual per solder paste is recommended. It was found that underlying flux systems can lead to changes in release properties in stencil printing process.

Electromigration

Electromigration was not observed in this study. Care should be taken for high current transmitting packages.

Units

If not otherwise stated, all measurement units given in this document are metric units. This means that also the package nomenclature, i.e. the term “0603”, refers to metric units.

9. Revision history

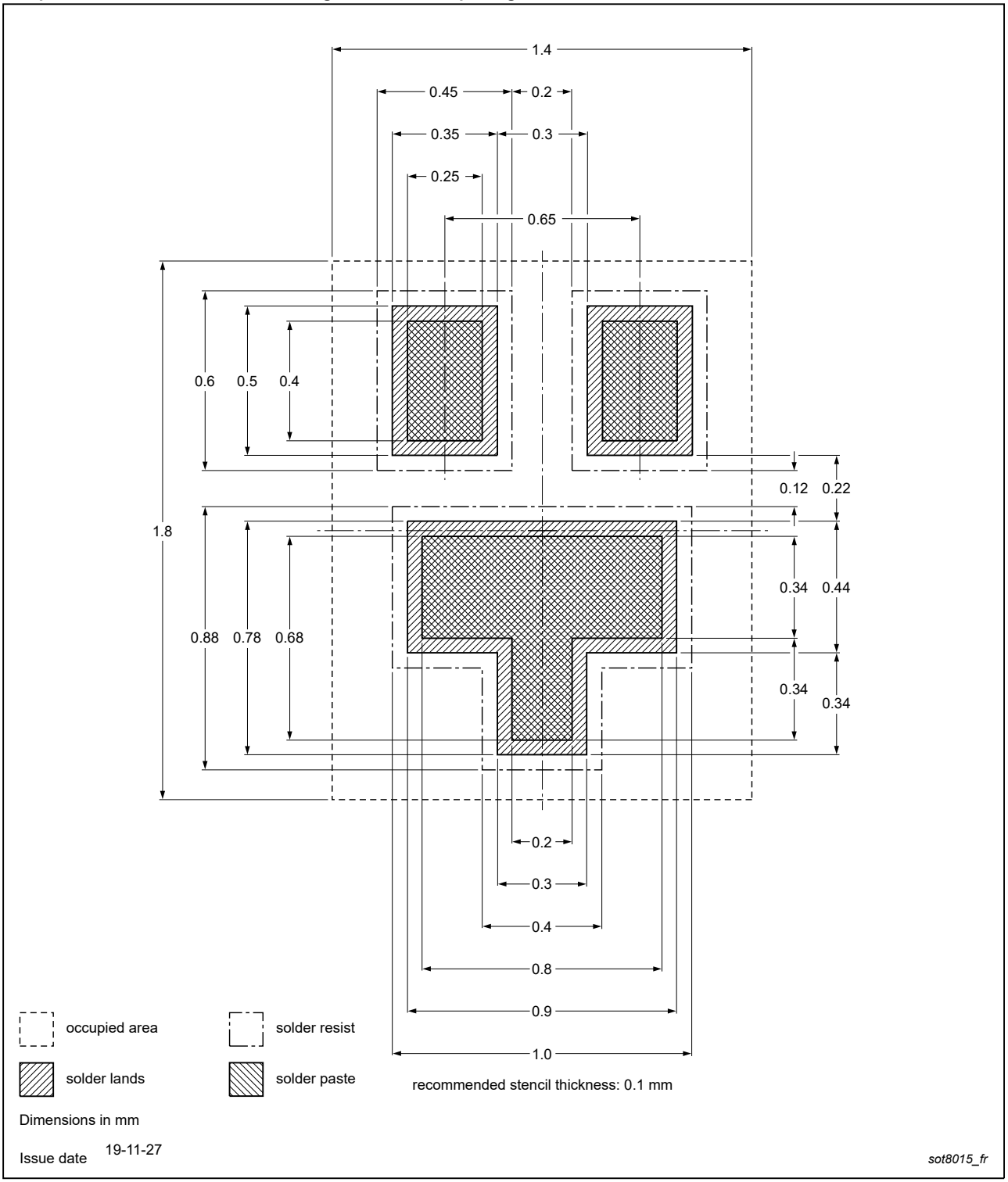
Table 5. Revision history

Revision number	Date	Description
1.1	2022-02-22	DSN0603 footprint drawing updated in Fig. 2.
1.0	2022-02-18	Initial version.

10. Appendix 1: reflow soldering footprints

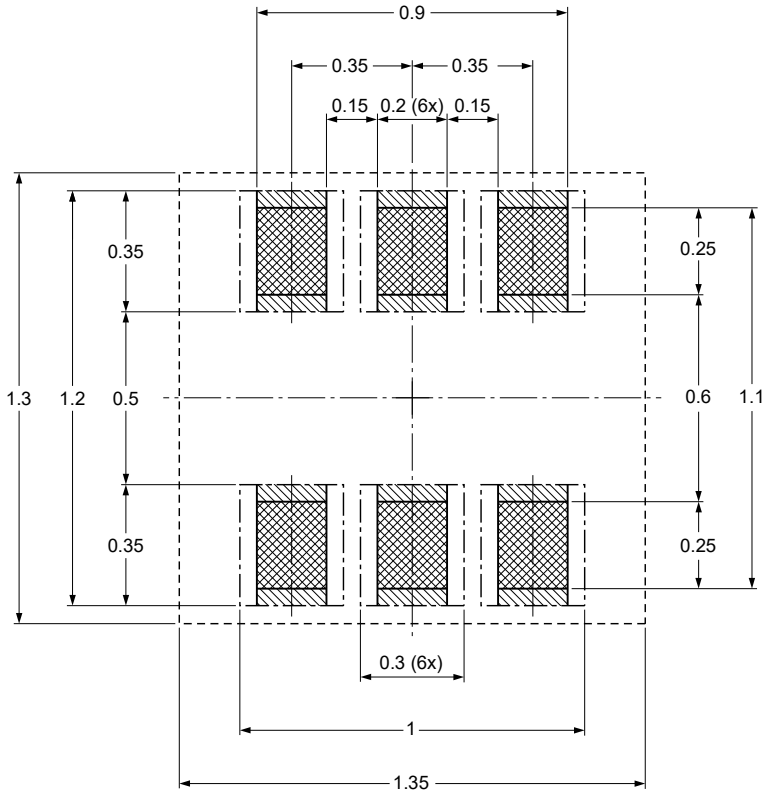
DFN1110D-3

Footprint information for reflow soldering of DFN1110D-3 package **SOT8015**



DFN1010B-6

Footprint information for reflow soldering of DFN1010B-6 package **SOT1216**



solder paste

solder land plus solder paste

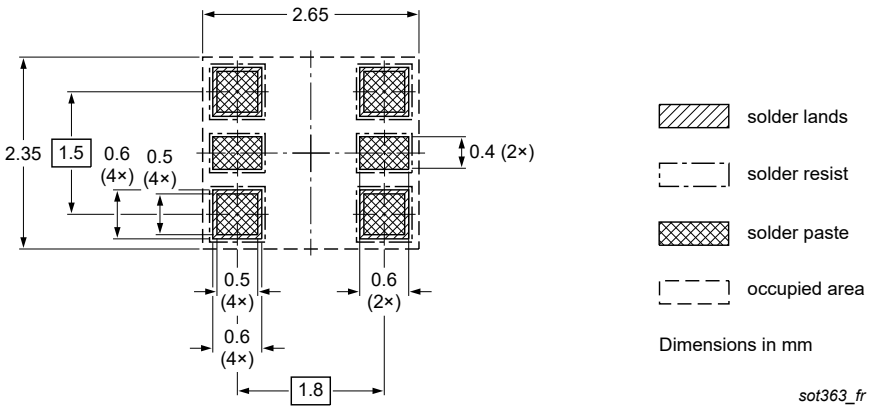
occupied area

solder resist

Dimensions in mm

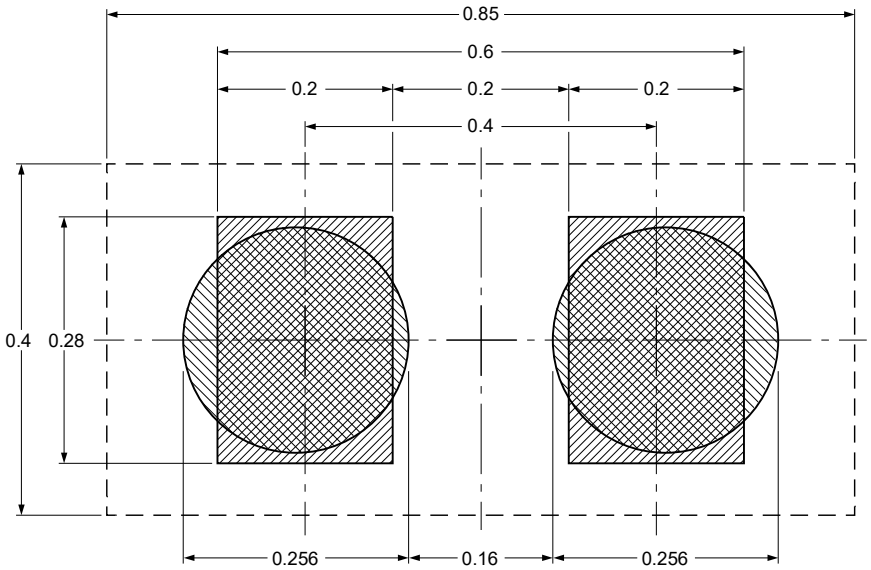
Issue date ~~14-07-28~~ 17-03-31

sot1216_fr



DSN0603

Footprint information for reflow soldering of leadless ultra small package; 2 terminals **SOD962**



recommended stencil thickness: 0.1 mm

occupied area

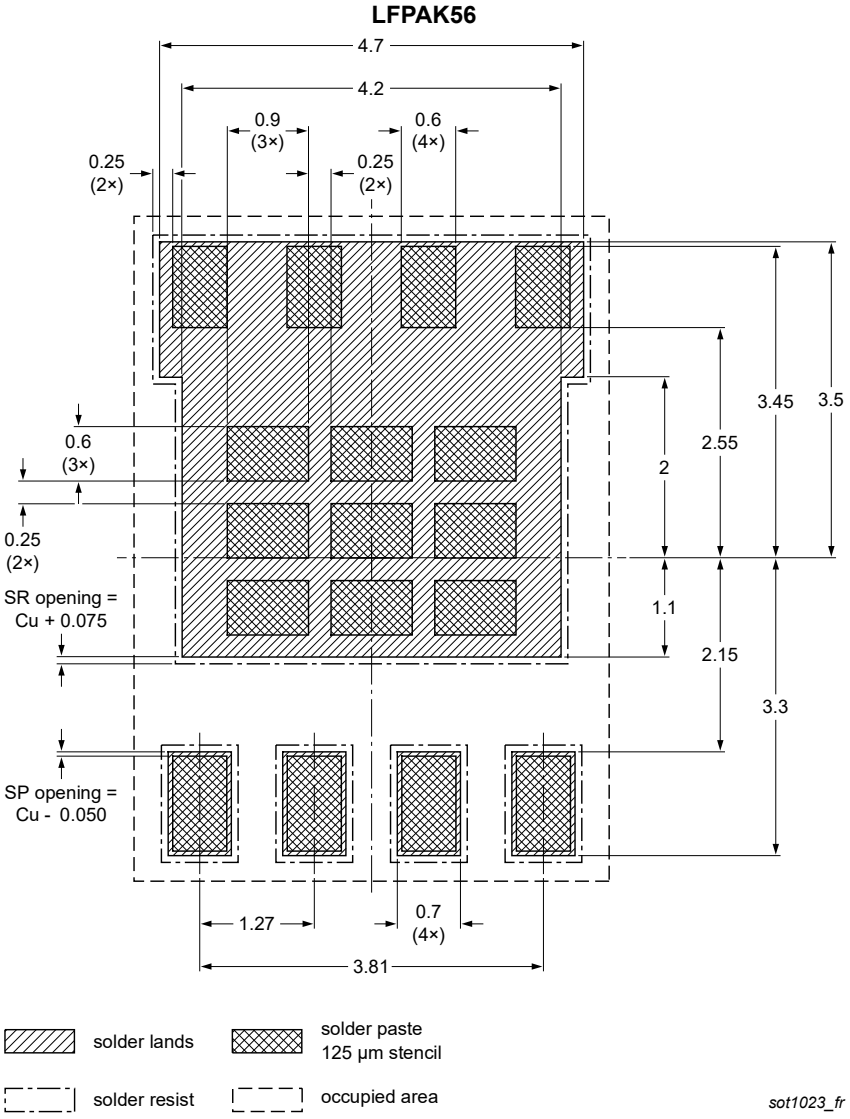
solder paste

solder lands

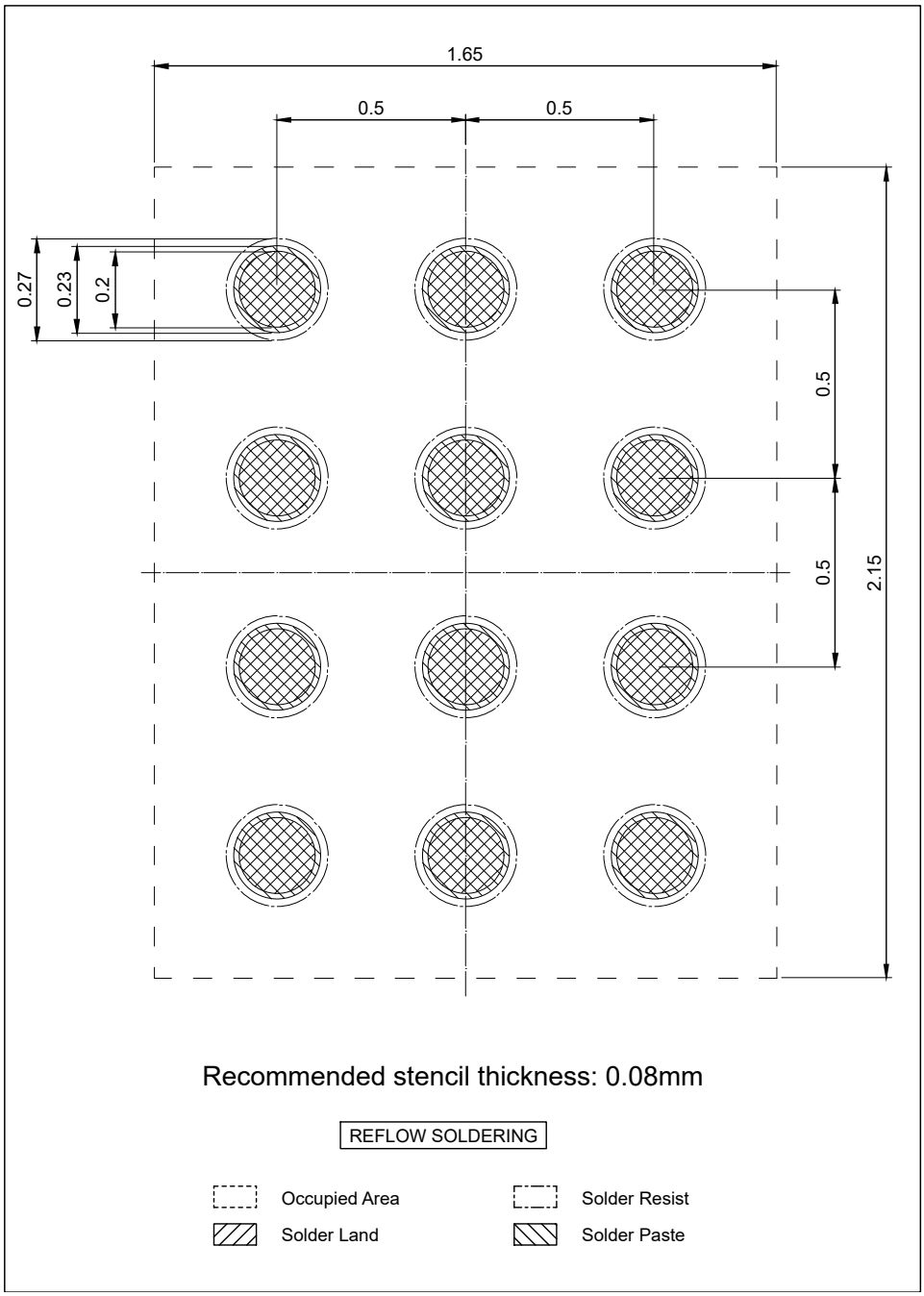
Dimensions in mm

Issue date ~~16-01-26~~ 20-09-15

sod962_fr



WLCSP12



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