74LV4060-Q100

14-stage binary ripple counter with oscillator

Rev. 3 — 16 April 2024 | Product data sheet

1. General description

The 74LV4060-Q100 is a 14-stage ripple-carry counter/divider and oscillator with three oscillator terminals (RS, R_{TC} and C_{TC}), ten buffered parallel outputs (Q_3 to Q_9 and Q_{11} to Q_{13}) and an overriding asynchronous master reset (MR). The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. In this case, keep the oscillator pins (R_{TC} and C_{TC}) floating. The counter advances on the HIGH-to-LOW transition of RS. A HIGH level on MR clears all counter stages and forces all outputs LOW, independent of the other input conditions. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess V_{CC}.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.0 V to 5.5 V
- Optimized for low voltage applications from 1.0 V to 3.6 V
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V; T_{amb} = 25 °C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V; T_{amb} = 25 °C
- All active components on chip
- RC or crystal oscillator configuration
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Applications

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV4060D-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

nexperia

Type number	Package			
	Temperature range	Name	Description	Version
74LV4060PW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram

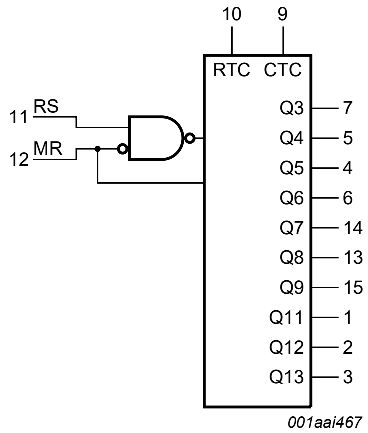


Fig. 1. Logic symbol

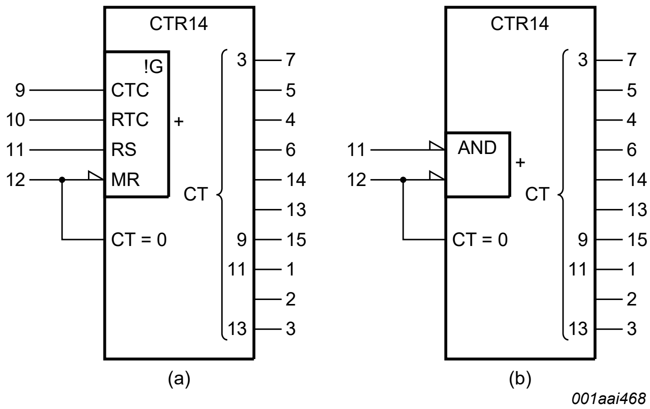


Fig. 2. IEC logic symbol

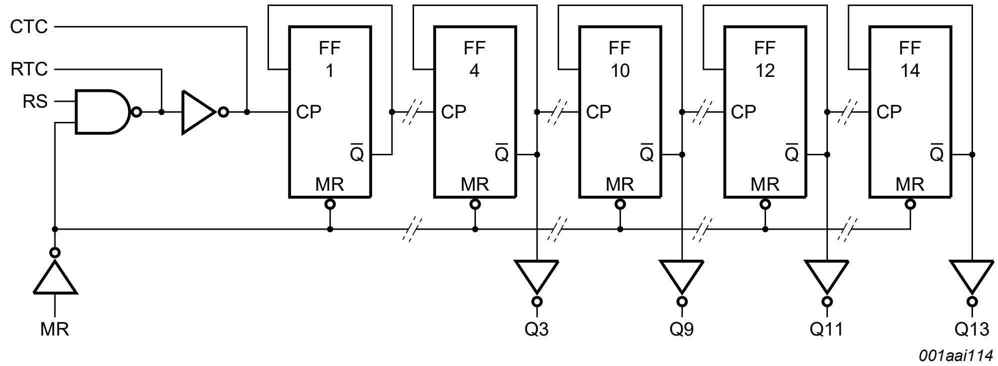


Fig. 3. Logic diagram

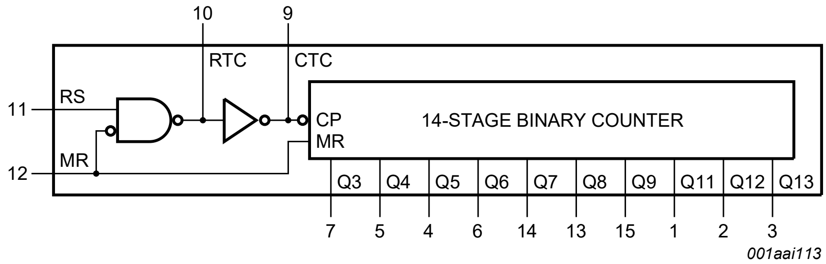
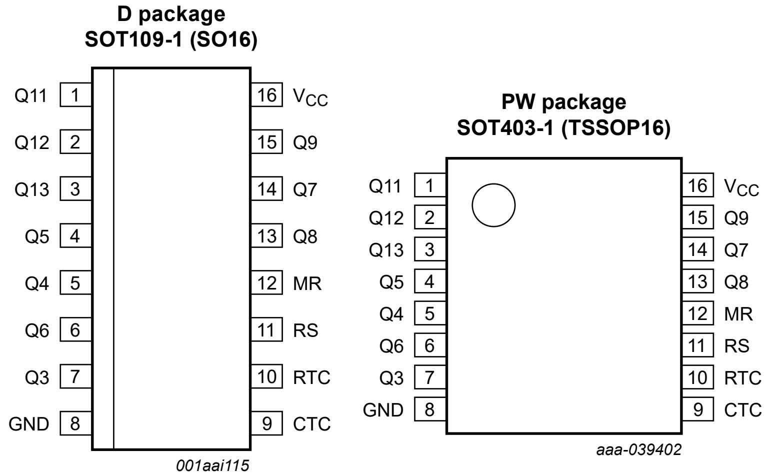


Fig. 4. Functional diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q11 to Q13	1, 2, 3	counter output
Q3 to Q9	7, 5, 4, 6, 14, 13, 15	counter output
GND	8	ground (0 V)
CTC	9	external capacitor connection
RTC	10	external resistor connection
RS	11	clock input/oscillator pin
MR	12	master reset
V_{CC}	16	supply voltage

7. Functional description

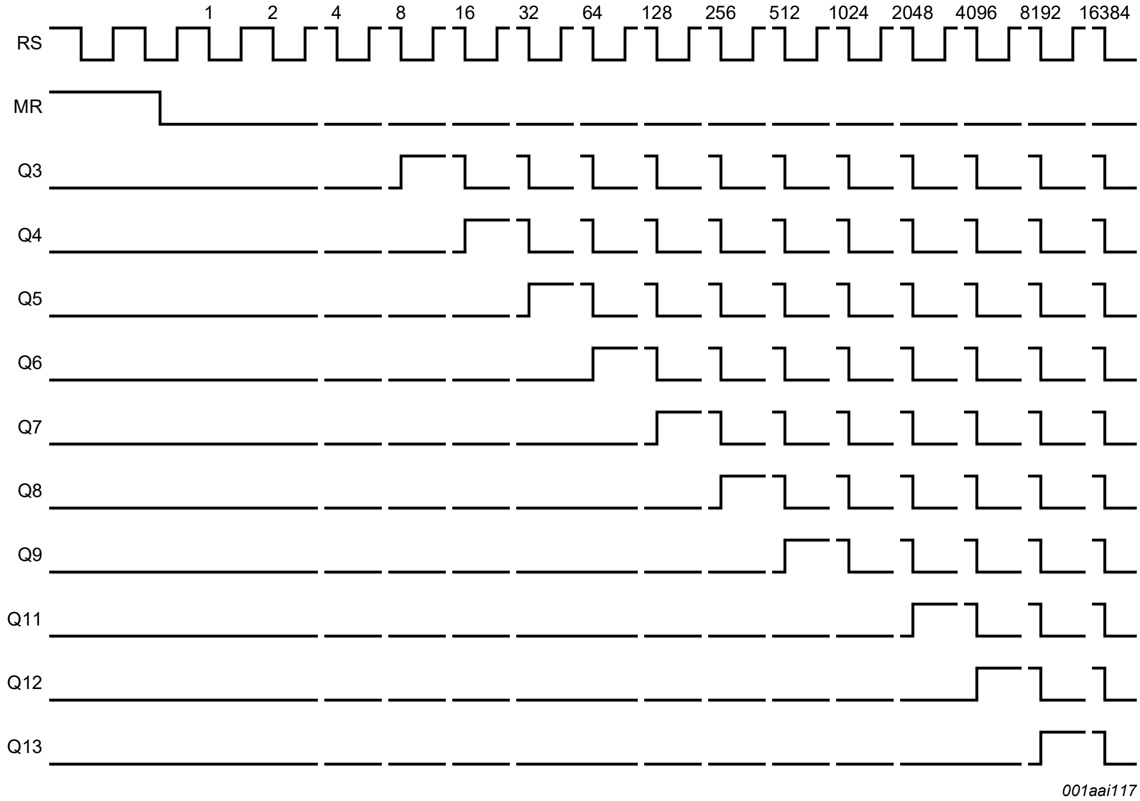


Fig. 5. Timing diagram

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V [1]	-	±20	mA
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{CC} + 0.5 V [1]	-	±50	mA
I_O	output current	-0.5 V < V_O < V_{CC} + 0.5 V	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

9. Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	[1]	1.0	3.3	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.0 V to 2.0 V	-	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V	-	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V	-	-	100	ns/V
		V_{CC} = 3.6 V to 5.5 V	-	-	50	ns/V

[1] The 74LV4060-Q100 is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V.

10. Static characteristics

Table 5. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	MR input						
		V_{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V_{CC} = 2.0 V	1.4	-	-	1.4	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V to 5.5 V	$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
		RS input						
		V_{CC} = 1.2 V	1.0	-	-	1.0	-	V
		V_{CC} = 2.0 V	1.6	-	-	1.6	-	V
		V_{CC} = 2.7 V to 3.6 V	2.4	-	-	2.4	-	V
		V_{CC} = 4.5 V to 5.5 V	$0.8V_{CC}$	-	-	$0.8V_{CC}$	-	V
V_{IL}	LOW-level input voltage	MR input						
		V_{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V_{CC} = 2.0 V	-	-	0.6	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	V
		RS input						
		V_{CC} = 1.2 V	-	-	0.2	-	0.2	V
		V_{CC} = 2.0 V	-	-	0.4	-	0.4	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.5	-	0.5	V
		V_{CC} = 4.5 V to 5.5 V	-	-	$0.2V_{CC}$	-	$0.2V_{CC}$	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{OH}	HIGH-level output voltage	RTC output; RS = MR = GND						
		V_{CC} = 1.2 V; I_O = -3.4 mA	-	-	-	-	-	V
		V_{CC} = 2.0 V; I_O = -3.4 mA	-	-	-	-	-	V
		V_{CC} = 2.7 V; I_O = -3.4 mA	-	-	-	-	-	V
		V_{CC} = 3.0 V; I_O = -3.4 mA	2.40	2.82	-	2.20	-	V
		V_{CC} = 4.5 V; I_O = -3.4 mA	-	-	-	-	-	V
		RTC output; RS = MR = V_{CC}						
		V_{CC} = 1.2 V; I_O = -0.8 mA	-	-	-	-	-	V
		V_{CC} = 2.0 V; I_O = -0.8 mA	-	-	-	-	-	V
		V_{CC} = 2.7 V; I_O = -0.8 mA	-	-	-	-	-	V
		V_{CC} = 3.0 V; I_O = -0.8 mA	2.40	2.82	-	2.20	-	V
		V_{CC} = 4.5 V; I_O = -0.8 mA	-	-	-	-	-	V
V_{OH}	HIGH-level output voltage	RTC output; RS = MR = GND						
		V_{CC} = 1.2 V; I_O = -100 μA	1.0	1.2	-	1.0	-	V
		V_{CC} = 2.0 V; I_O = -100 μA	1.8	2.0	-	1.8	-	V
		V_{CC} = 2.7 V; I_O = -100 μA	-	-	-	-	-	V
		V_{CC} = 3.0 V; I_O = -100 μA	2.8	3.0	-	2.8	-	V
		V_{CC} = 4.5 V; I_O = -100 μA	-	-	-	-	-	V
		RTC output; RS = MR = V_{CC}						
		V_{CC} = 1.2 V; I_O = -100 μA	1.0	1.2	-	1.0	-	V
		V_{CC} = 2.0 V; I_O = -100 μA	1.8	2.0	-	1.8	-	V
		V_{CC} = 2.7 V; I_O = -100 μA	-	-	-	-	-	V
		V_{CC} = 3.0 V; I_O = -100 μA	2.8	3.0	-	2.8	-	V
		V_{CC} = 4.5 V; I_O = -100 μA	-	-	-	-	-	V
		CTC output; RS = V_{IH} and MR = V_{IL}						
		V_{CC} = 1.2 V; I_O = -3.8 mA	-	1.2	-	-	-	V
		V_{CC} = 2.0 V; I_O = -3.8 mA	-	-	-	-	-	V
		V_{CC} = 2.7 V; I_O = -3.8 mA	-	-	-	-	-	V
		V_{CC} = 3.0 V; I_O = -3.8 mA	2.40	2.82	-	2.20	-	V
		V_{CC} = 4.5 V; I_O = -3.8 mA	-	-	-	-	-	V
		except RTC output; V_I = V_{IH} or V_{IL}						
		V_{CC} = 1.2 V; I_O = -100 μA	1.0	1.2	-	1.0	-	V
		V_{CC} = 2.0 V; I_O = -100 μA	1.8	2.0	-	1.8	-	V
		V_{CC} = 2.7 V; I_O = -100 μA	-	-	-	-	-	V
		V_{CC} = 3.0 V; I_O = -100 μA	2.8	3.0	-	2.8	-	V
		V_{CC} = 4.5 V; I_O = -100 μA	-	-	-	-	-	V
		except RTC and CTC outputs; V_I = V_{IH} or V_{IL}						
		V_{CC} = 1.2 V; I_O = -6 mA	-	-	-	-	-	V
		V_{CC} = 2.0 V; I_O = -6 mA	-	-	-	-	-	V
		V_{CC} = 2.7 V; I_O = -6 mA	-	-	-	-	-	V
		V_{CC} = 3.0 V; I_O = -6 mA	2.40	2.82	-	2.20	-	V
		V_{CC} = 4.5 V; I_O = -6 mA	-	-	-	-	-	V

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{OL}	LOW-level output voltage	RTC output; RS = V_{CC} and MR = GND						
		V_{CC} = 1.2 V; I_O = -3.4 mA	-	-	-	-	-	V
		V_{CC} = 2.0 V; I_O = -3.4 mA	-	-	-	-	-	V
		V_{CC} = 2.7 V; I_O = -3.4 mA	-	-	-	-	-	V
		V_{CC} = 3.0 V; I_O = -3.4 mA	-	0.25	0.40	-	0.50	V
		V_{CC} = 4.5 V; I_O = -3.4 mA	-	-	-	-	-	V
V_{OL}	LOW-level output voltage	RTC output; RS = V_{CC} and MR = GND;						
		V_{CC} = 1.2 V; I_O = -100 μA	-	0	0.2	-	0.2	V
		V_{CC} = 2.0 V; I_O = -100 μA	-	0	0.2	-	0.2	V
		V_{CC} = 2.7 V; I_O = -100 μA	-	-	-	-	-	V
		V_{CC} = 3.0 V; I_O = -100 μA	-	0	0.2	-	0.2	V
		V_{CC} = 4.5 V; I_O = -100 μA	-	-	-	-	-	V
		CTC output; RS = V_{IH} and MR = V_{IL};						
		V_{CC} = 1.2 V; I_O = -3.8 mA	-	-	-	-	-	V
		V_{CC} = 2.0 V; I_O = -3.8 mA	-	-	-	-	-	V
		V_{CC} = 2.7 V; I_O = -3.8 mA	-	-	-	-	-	V
		V_{CC} = 3.0 V; I_O = -3.8 mA	-	0.25	-	0.40	0.50	V
		V_{CC} = 4.5 V; I_O = -3.8 mA	-	-	-	-	-	V
		except RTC output; V_I = V_{IH} or V_{IL};						
		V_{CC} = 1.2 V; I_O = -100 μA	-	0	0.2	-	0.2	V
		V_{CC} = 2.0 V; I_O = -100 μA	-	0	0.2	-	0.2	V
		V_{CC} = 2.7 V; I_O = -100 μA	-	-	-	-	-	V
		V_{CC} = 3.0 V; I_O = -100 μA	-	0	0.2	-	0.2	V
		V_{CC} = 4.5 V; I_O = -100 μA	-	-	-	-	-	V
		except RTC and CTC output; V_I = V_{IH} or V_{IL}						
		V_{CC} = 1.2 V; I_O = -6 mA	-	-	-	-	-	V
		V_{CC} = 2.0 V; I_O = -6 mA	-	-	-	-	-	V
		V_{CC} = 2.7 V; I_O = -6 mA	-	0.25	0.40	-	0.50	V
		V_{CC} = 3.0 V; I_O = -6 mA	-	-	-	-	-	V
		V_{CC} = 4.5 V; I_O = -6 mA	-	-	-	-	-	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND	-	-	1.0	-	1.0	μA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	-	20	-	160	μA
		V_{CC} = 5.5 V; V_I = V_{CC} or GND; I_O = 0 A	-	-	-	-	80	μA
ΔI_{CC}	additional supply current	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} - 0.6 V; I_O = 0 A	-	-	500	-	850	μA
C_I	input capacitance		-	3.5	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 6. Dynamic characteristics

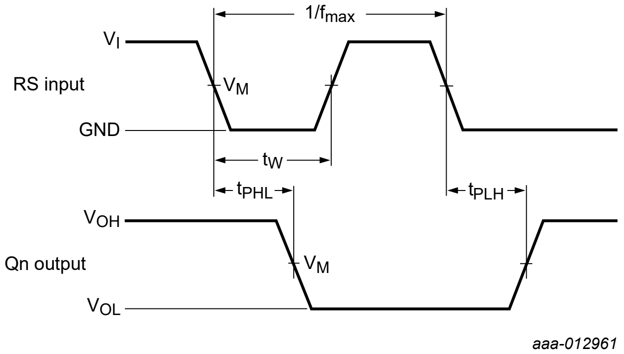
GND = 0 V; for test circuit, see Fig. 9.

Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	RS to Q3; see Fig. 6 and Fig. 8	[2]						
		V_{CC} = 1.2 V		-	180	-	-	-	ns
		V_{CC} = 2.0 V		-	52	84	-	105	ns
		V_{CC} = 2.7 V		-	42	66	-	83	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	29	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	33	53	-	66	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	-	24	39	-	49	ns
		Qn to Qn+1; see Fig. 7 and Fig. 8							
		V_{CC} = 1.2 V		-	40	-	-	-	ns
		V_{CC} = 2.0 V		-	14	23	-	29	ns
		V_{CC} = 2.7 V		-	10	16	-	20	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	6	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	8	13	-	16	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	-	6	9	-	11	ns
t_{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 7 and Fig. 8							
		V_{CC} = 1.2 V		-	100	-	-	-	ns
		V_{CC} = 2.0 V		-	29	46	-	58	ns
		V_{CC} = 2.7 V		-	24	39	-	49	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	16	-	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	19	31	-	39	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	-	14	23	-	29	ns
t_W	pulse width	RS HIGH or LOW; see Fig. 6							
		V_{CC} = 2.0 V		34	9	-	38	-	ns
		V_{CC} = 2.7 V		25	6	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	20	5	-	24	-	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	16	4	-	20	-	ns
		MR HIGH; see Fig. 8							
		V_{CC} = 2.0 V		34	10	-	38	-	ns
		V_{CC} = 2.7 V		25	8	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	20	6	-	24	-	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	16	4	-	20	-	ns
t_{rec}	recovery time	MR to RS; see Fig. 8							
		V_{CC} = 2.0 V		29	18	-	37	-	ns
		V_{CC} = 2.7 V		26	16	-	32	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	18	11	-	23	-	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	12	7	-	15	-	ns

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
f_{max}	maximum frequency	see Fig. 6						
		V_{CC} = 2.0 V	14	40	-	9	-	MHz
		V_{CC} = 2.7 V	19	70	-	12	-	MHz
		V_{CC} = 3.3 V; C_L = 15 pF	-	99	-	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V [3]	24	90	-	15	-	MHz
		V_{CC} = 4.5 V to 5.5 V [4]	30	100	-	19	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} [5]	-	40	-	-	-	pF

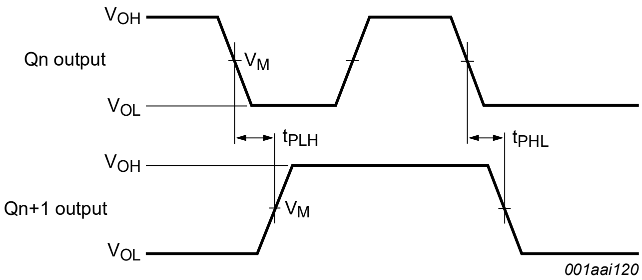
[1] All typical values are measured at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
[3] Typical value measured at V_{CC} = 3.3 V.
[4] Typical value measured at V_{CC} = 5.0 V.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit



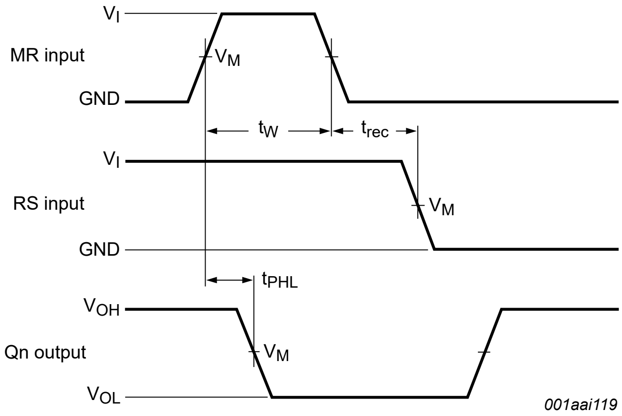
Measurement points are given in Table 7.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. Waveforms showing the clock (RS) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum frequency



Measurement points are given in Table 7.
V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Waveforms showing the output Qn to output Qn+1 propagation delays



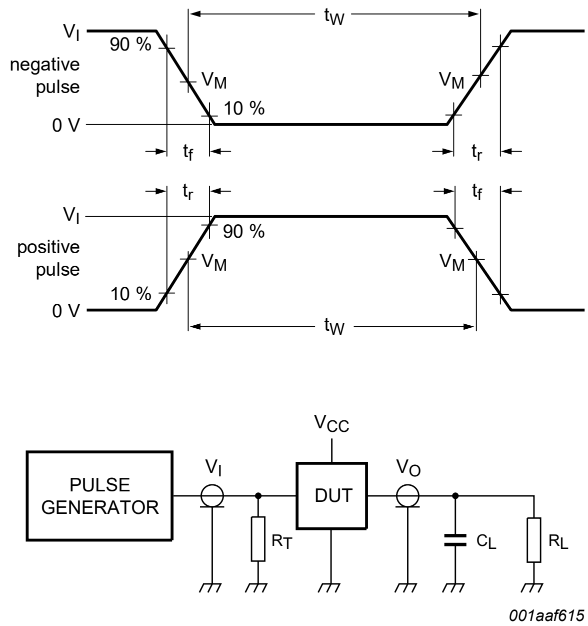
Measurement points are given in Table 7.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. Waveforms showing the master reset (MR) pulse width, the master reset to output (Qn) propagation delays and the master reset to clock (RS) recovery time

Table 7. Measurement points

Supply voltage	Input	Output
V_{CC}	**V_M**	**V_M**
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V
≥ 4.5 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 8.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

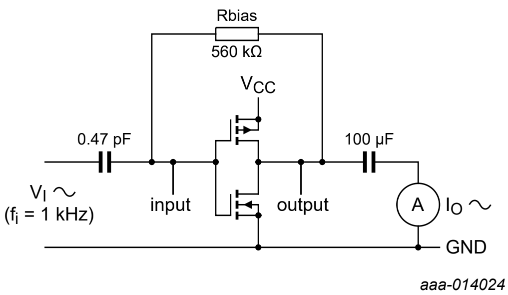
R_L = Load resistance.

Fig. 9. Test circuit for measuring switching times

Table 8. Test data

Supply voltage	Input		Load	
V_{CC}	V_I	t_r, t_f	C_L	R_L
V_{CC} < 2.7 V	V_{CC}	2.5 ns	50 pF	1 kΩ
2.7 V < V_{CC} < 3.6 V	2.7 V	2.5 ns	15 pF, 50 pF	1 kΩ
V_{CC} ≥ 4.5 V	V_{CC}	2.5 ns	50 pF	1 kΩ

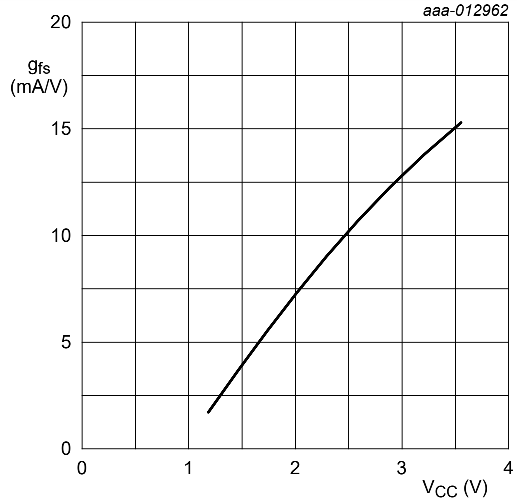
12. Typical forward transconductance



$g_{fs} = \Delta I_O / \Delta V_I$ at V_O is constant; MR = LOW

See Fig. 11.

Fig. 10. Test setup for measuring forward transconductance



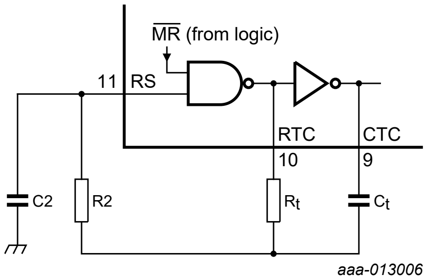
T_{amb} = 25 °C

Fig. 11. Typical forward transconductance as function of the supply voltage

13. RC oscillator

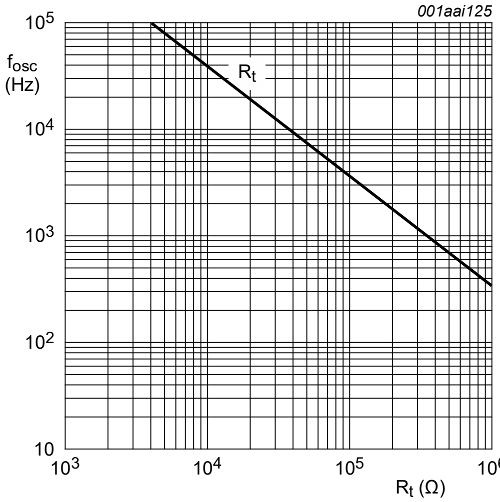
13.1. Timing component limitations

The oscillator frequency is mainly determined by $R_t \times C_t$, provided R2 ≈ $2R_t$ and R2 x C2 is much less than R_t x C_t. The function of R2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the 'ON' resistance in series with it, which typically is 280 Ω at V_{CC} = 1.2 V, 130 Ω at V_{CC} = 2.0 V and 100 Ω at V_{CC} 3.0 V. The recommended values for these components to maintain agreement with the typical oscillation formula are: C_t > 50 pF, up to any practical value, 10 kΩ < R_t < 1 MΩ. In order to avoid start-up problems, R_t ≥ 1 kΩ.



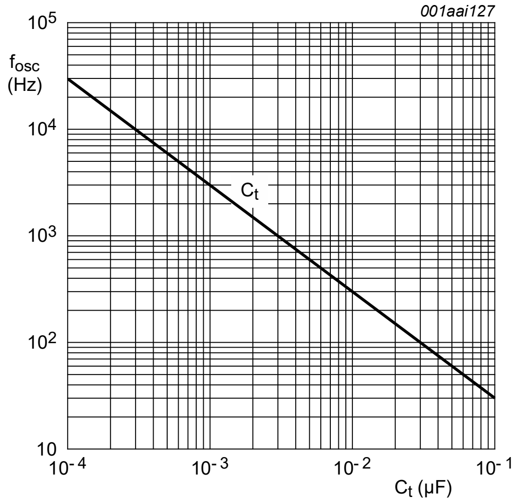
Typical formula for oscillator frequency: $f_{osc} = \frac{1}{2.5 \times R_t \times C_t}$

Fig. 12. Example of an RC oscillator



V_{CC} = 1.2 V to 3.6 V; T_{amb} = 25 °C
R_t curve: C_t = 1 nF; R2 = 2 × R_t

Fig. 13. RC oscillator frequency as a function of R_t



V_{CC} = 1.2 V to 3.6 V; T_{amb} = 25 °C
C_t curve: R_t = 100 kΩ; R2 = 200 kΩ

Fig. 14. RC oscillator frequency as a function of C_t

13.2. Typical crystal oscillator circuit

In Fig. 15, R2 is the power limiting resistor. For starting and maintaining oscillation, a minimum transconductance is necessary, so R2 must not be too large. A practical value for R2 is 2.2 kΩ.

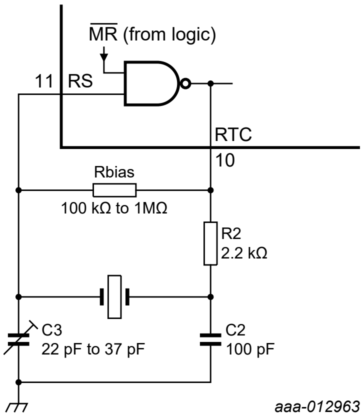
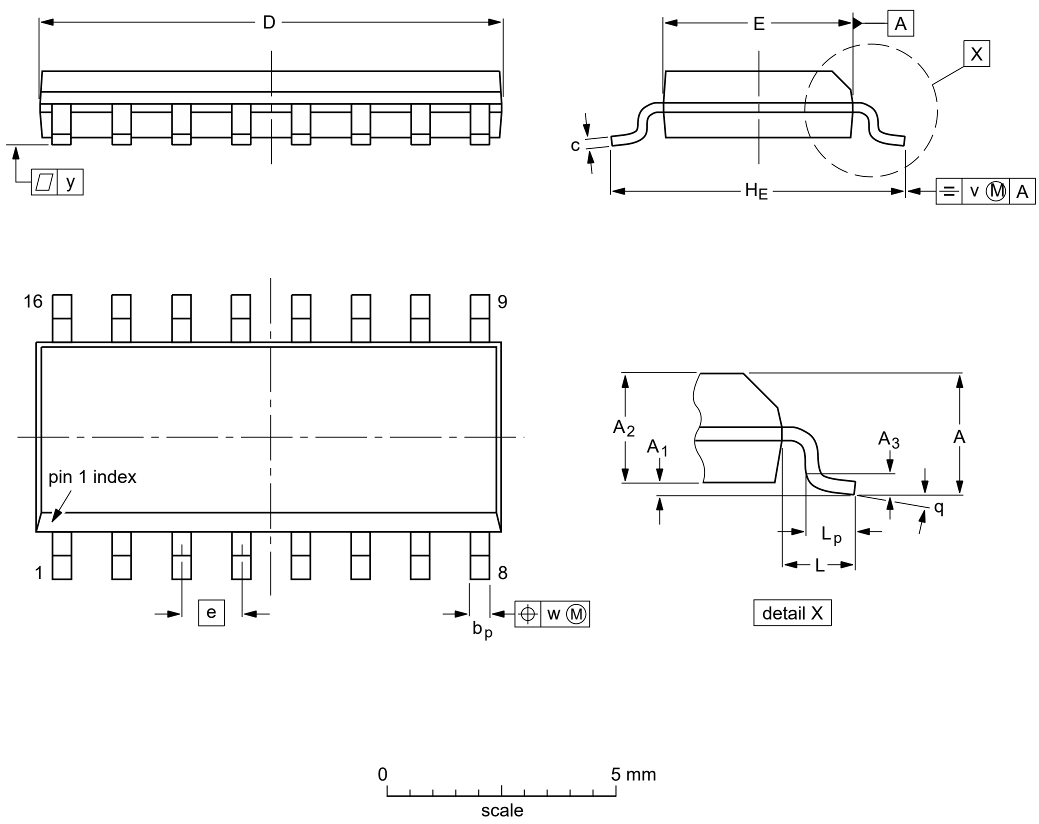


Fig. 15. External components connection for a typical crystal oscillator

14. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

Note

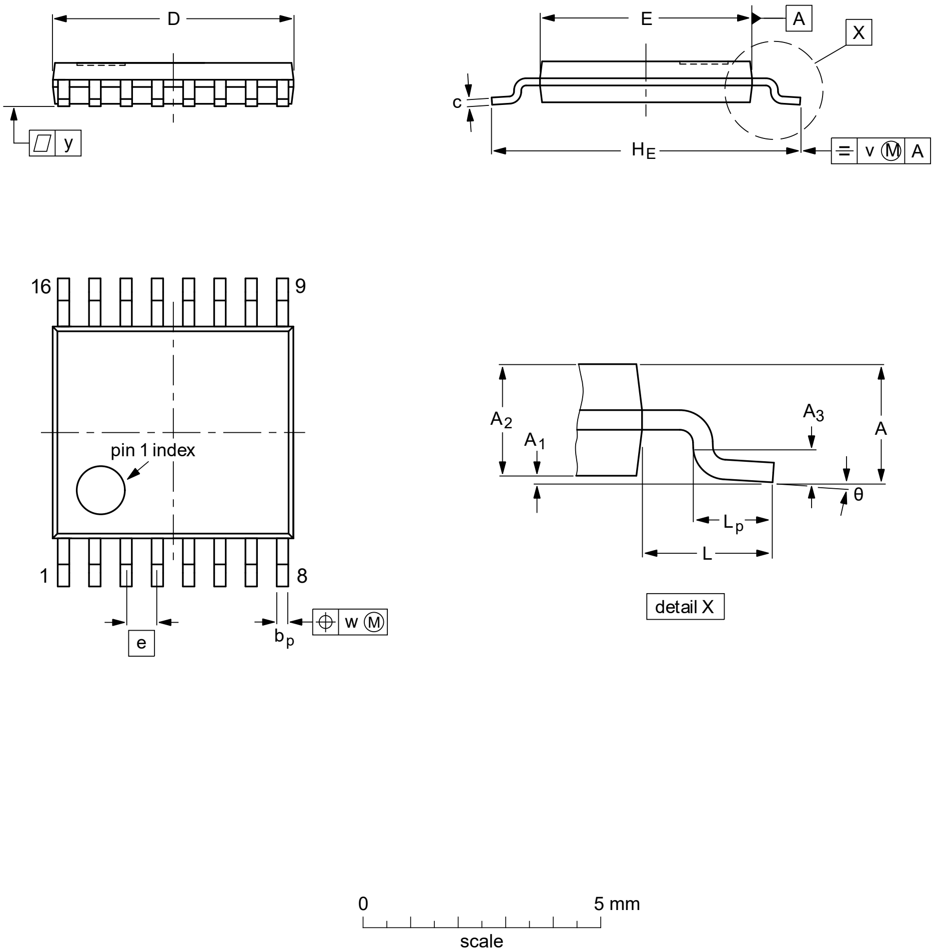
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 16. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 17. Package outline SOT403-1 (TSSOP16)

15. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

16. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV4060_Q100 v.3	20240416	Product data sheet	-	74LV4060_Q100 v.2
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Section 14: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153			
74LV4060_Q100 v.2	20210324	Product data sheet	-	74LV4060_Q100 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Section 8: Derating values for P_{tot} total power dissipation updated.			
74LV4060_Q100 v.1	20140725	Product data sheet	-	-

17. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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