74LVC2G126-Q100

Bus buffer/line driver; 3-state Rev. 5 — 17 August 2023

## 1. General description

The 74LVC2G126-Q100 is a dual buffer/line driver with 3-state outputs controlled by the output enable inputs (nOE). Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)

  Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- ±24 mA output drive (V<sub>CC</sub> = 3.0 V)
- CMOS low power consumption
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

## 3. Ordering information

## Table 1. Ordering information

Type number	Package					
	Temperature range	Name	Description	Version		
74LVC2G126DP-Q100	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	<u>SOT505-2</u>		
74LVC2G126DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	<u>SOT765-1</u>		

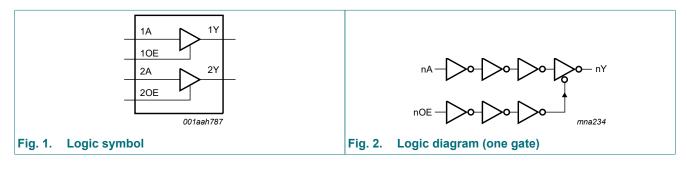
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# 4. Marking

Table 2. Marking codes			
Type number	Marking code [1]		
74LVC2G126DP-Q100	V26		
74LVC2G126DC-Q100	V26		

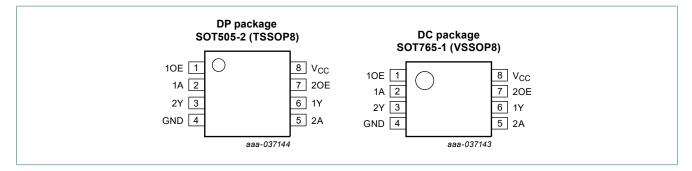
[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

# 5. Functional diagram



# 6. Pinning information

## 6.1. Pinning



## 6.2. Pin description

Table 3. Pin description					
Symbol	Pin	Description			
10E, 20E	1, 7	output enable input (active HIGH)			
1A, 2A	2, 5	data input			
1Y, 2Y	6, 3	data output			
GND	4	ground (0 V)			
V <sub>CC</sub>	8	supply voltage			

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# 7. Functional description

#### Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input nOE nA		Output
nOE	nA	nY
Н	L	L
Н	Н	Н
L	X	Z

## 8. Limiting values

## Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Mir	n	Мах	Unit
V <sub>CC</sub>	supply voltage		-0.	5	+6.5	V
I <sub>IK</sub>	input clamping current	V <sub>1</sub> < 0 V	-50	)	-	mA
VI	input voltage	[1	] -0.9	5	+6.5	V
I <sub>OK</sub>	output clamping current	$V_{\rm O}$ > $V_{\rm CC}$ or $V_{\rm O}$ < 0 V	-		±50	mA
Vo	output voltage	Active mode [1	] -0.9	5	V <sub>CC</sub> + 0.5	V
		Power-down mode; $V_{CC} = 0 V$ [1	] -0.	5	+6.5	V
I <sub>O</sub>	output current	$V_{O} = 0 V$ to $V_{CC}$	-		±50	mA
I <sub>CC</sub>	supply current		-		+100	mA
I <sub>GND</sub>	ground current		-10	0	-	mA
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40 \text{ °C to } +125 \text{ °C}$ [2	] -		250	mW
T <sub>stg</sub>	storage temperature		-65	5	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT505-2 (TSSOP8) package: P<sub>tot</sub> derates linearly with 4.6 mW/K above 96 °C.

For SOT765-1 (VSSOP8) package: Ptot derates linearly with 4.9 mW/K above 99 °C.

# 9. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		1.65	5.5	V
VI	input voltage		0	5.5	V
Vo	output voltage	Active mode	0	V <sub>CC</sub>	V
		Power-down mode; $V_{CC} = 0 V$	0	5.5	V
T <sub>amb</sub>	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.65 V to 2.7 V	-	20	ns/V
		V <sub>CC</sub> = 2.7 V to 5.5 V	-	10	ns/V

# **10. Static characteristics**

## Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol Parameter		Conditions	-40	-40 °C to +85 °C			-40 °C to +125 °C		
			Min	Min Typ [1]		Min Max			
VIH	HIGH-level	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65V <sub>CC</sub>	-	-	0.65V <sub>CC</sub>	-	V	
	input voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V	
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V	
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7V <sub>CC</sub>	-	-	0.7V <sub>CC</sub>	-	V	
V <sub>IL</sub>	LOW-level input	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	$0.35V_{CC}$	-	$0.35V_{CC}$	V	
	voltage	V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V	
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V	
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3V <sub>CC</sub>	-	0.3V <sub>CC</sub>	V	
V <sub>OL</sub>	LOW-level	$V_{I} = V_{IH} \text{ or } V_{IL}$							
	output voltage	I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	0.1	-	0.1	V	
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	-	0.70	V	
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.3	-	0.45	V	
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	-	0.60	V	
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	-	0.80	V	
		I <sub>O</sub> = 32 mA; V <sub>CC</sub> = 4.5 V	-	-	0.55	-	0.80	V	
V <sub>OH</sub>	HIGH-level	$V_{I} = V_{IH} \text{ or } V_{IL}$							
	output voltage	I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 5.5 V	V <sub>CC</sub> - 0.1	-	-	V <sub>CC</sub> - 0.1	-	V	
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	0.95	-	V	
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.9	-	-	1.7	-	V	
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	1.9	-	V	
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.3	-	-	2.0	-	V	
		I <sub>O</sub> = -32 mA; V <sub>CC</sub> = 4.5 V	3.8	-	-	3.4	-	V	
I	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	±0.1	±1	-	±1	μA	
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND; V <sub>CC</sub> = 3.6 V	-	±0.1	±2	-	±2	μA	
I <sub>OFF</sub>	power-off leakage current	$V_{I} \text{ or } V_{O} = 5.5 \text{ V}; V_{CC} = 0 \text{ V}$	-	±0.1	±2	-	±2	μA	
I <sub>CC</sub>	supply current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 1.65 V to 5.5 V; I <sub>O</sub> = 0 A	-	0.1	4	-	4	μA	
ΔI <sub>CC</sub>	additional supply current	per pin; $V_I = V_{CC} - 0.6 \text{ V}$ ; $I_O = 0 \text{ A}$ ; $V_{CC} = 2.3 \text{ V}$ to 5.5 V	-	5	500	-	500	μA	
CI	input capacitance		-	2	-	-	-	pF	

[1] Typical values are measured at  $V_{CC}$  = 3.3 V and  $T_{amb}$  = 25  $^\circ C.$ 

# **11. Dynamic characteristics**

## Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

Symbol Parameter		Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	1
t <sub>pd</sub>	propagation delay	nA to nY; see Fig. 3 [2]						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	3.9	9.8	1.0	12.3	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	2.6	4.9	0.5	6.3	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.8	4.7	1.0	5.9	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	2.4	4.3	0.5	5.4	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	1.9	3.2	0.5	4.0	ns
t <sub>en</sub>	enable time	nOE to nY; see Fig. 4 [3]						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	4.1	10.0	1.0	12.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.6	5.0	1.0	6.3	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.8	4.7	1.0	5.9	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.4	4.1	1.0	5.1	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	1.8	3.1	0.5	3.9	ns
t <sub>dis</sub>	disable time	nOE to nY; see Fig. 4 [4]						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	3.3	12.6	1.0	15.4	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	1.9	5.7	0.5	7.5	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.0	4.8	1.5	6.2	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.5	4.4	1.0	5.7	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	1.8	3.3	0.5	4.4	ns
C <sub>PD</sub>	power dissipation	per buffer; $V_I$ = GND to $V_{CC}$ [5]						
	capacitance	output enabled	-	17	-	-	-	pF
		output disabled	-	5	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ 

[3]  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ 

 $[4] \quad t_{dis} \text{ is the same as } t_{PLZ} \text{ and } t_{PHZ}$ 

[5]  $C_{PD}$  is used to determine the dynamic power dissipation (P<sub>D</sub> in  $\mu$ W).

 $P_{D} = C_{PD} \times V_{CC}^{2} \times f_{i} \times N + \Sigma(C_{L} \times V_{CC}^{2} \times f_{o}) \text{ where:}$ 

 $f_i$  = input frequency in MHz;

 $f_o$  = output frequency in MHz;

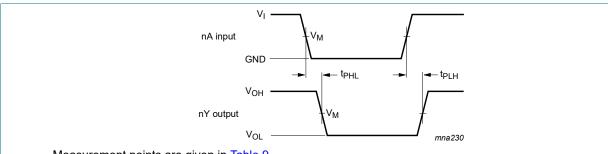
 $C_L$  = output load capacitance in pF;

 $V_{CC}$  = supply voltage in V;

N = number of inputs switching;  $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

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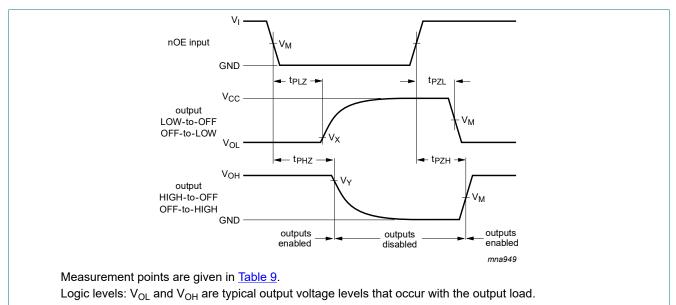




Measurement points are given in <u>Table 9</u>.

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

## Fig. 3. The data input (nA) to output (nY) propagation delays

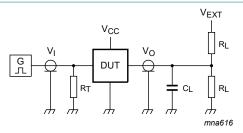


## Fig. 4. 3-state enable and disable times

Table 9. Measureme	Table 9. Measurement points						
Supply voltage	Input	Output	Output				
V <sub>cc</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>			
1.65 V to 1.95 V	0.5 × V <sub>CC</sub>	$0.5 \times V_{CC}$	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V			
2.3 V to 2.7 V	0.5 × V <sub>CC</sub>	$0.5 \times V_{CC}$	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V			
2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V			
3.0 V to 3.6 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V			
4.5 V to 5.5 V	0.5 × V <sub>CC</sub>	$0.5 \times V_{CC}$	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V			

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## Bus buffer/line driver; 3-state



Test data is given in Table 10.

Definitions for test circuit:

R<sub>L</sub> = Load resistance;

 $C_L$  = Load capacitance including jig and probe capacitance;

 $R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator;

 $V_{EXT}$  = External voltage for measuring switching times.

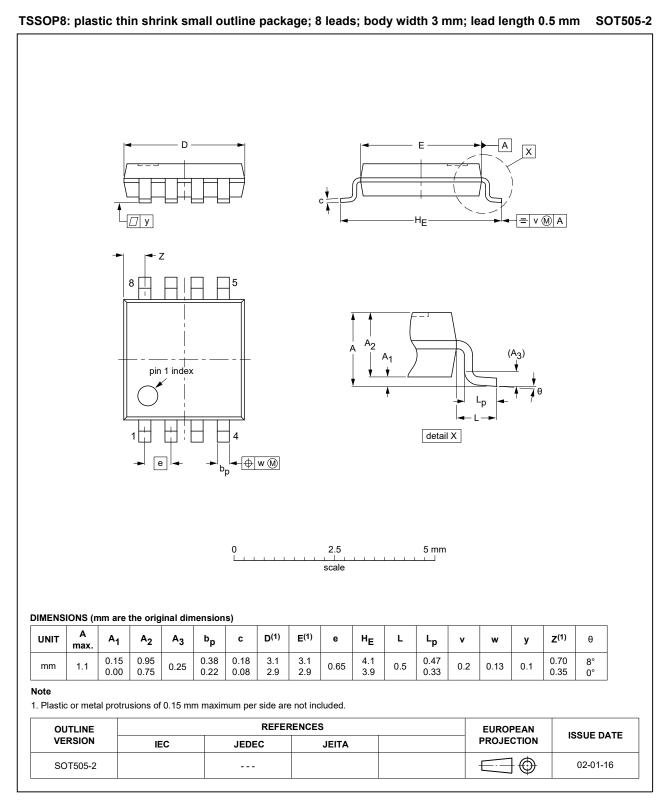
## Fig. 5. Test circuit for measuring switching times

## Table 10. Test data

Supply voltage	Input		Load		V <sub>EXT</sub>	V <sub>EXT</sub>		
V <sub>cc</sub>	VI	t <sub>r</sub> , t <sub>f</sub>	CL	RL	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>	
1.65 V to 1.95 V	V <sub>CC</sub>	≤ 2.0 ns	30 pF	1 kΩ	open	GND	$2 \times V_{CC}$	
2.3 V to 2.7 V	V <sub>CC</sub>	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2 \times V_{CC}$	
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V	
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V	
4.5 V to 5.5 V	V <sub>CC</sub>	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2 \times V_{CC}$	

## Bus buffer/line driver; 3-state

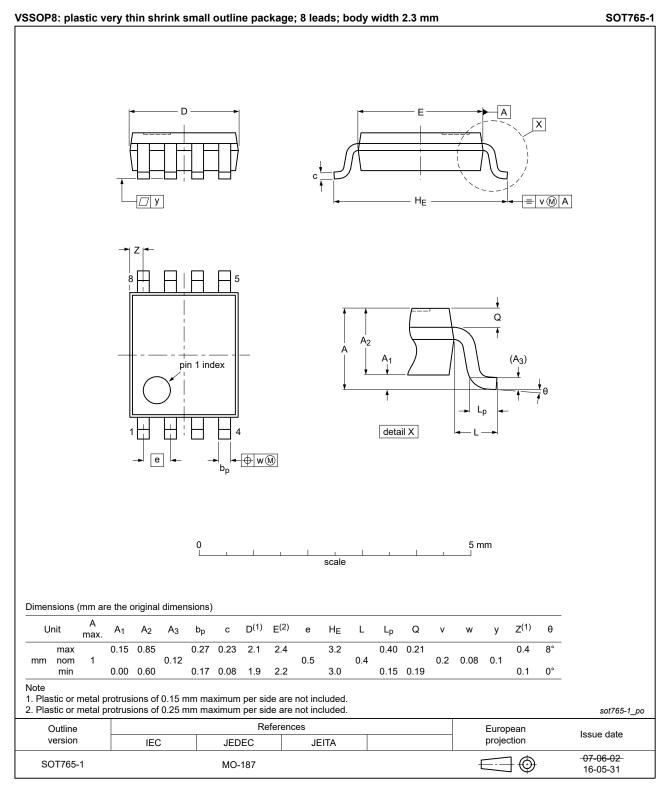
# 12. Package outline



## Fig. 6. Package outline SOT505-2 (TSSOP8)

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## Bus buffer/line driver; 3-state





# 13. Abbreviations

Table 11. Abbreviations					
Acronym	Description				
CDM	Charged Device Model				
CMOS	Complementary Metal-Oxide Semiconductor				
DUT	Device Under Test				
ESD	ElectroStatic Discharge				
НВМ	Human Body Model				
TTL	Transistor-Transistor Logic				

# 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC2G126_Q100 v.5	20230817	Product data sheet	-	74LVC2G126_Q100 v.4
Modifications:	• <u>Section 2</u> : E	SD specification updated a	according to the la	atest JEDEC standard.
74LVC2G126_Q100 v.4	20210428	Product data sheet	-	74LVC2G126_Q100 v.3
Modifications:		nd <u>Section 2</u> updated. Derating values for P <sub>tot</sub> total	power dissipation	n updated.
74LVC2G126_Q100 v.3	20190110	Product data sheet	-	74LVC2G126_Q100 v.2
Modifications:	guidelines o	of this data sheet has beer of Nexperia. have been adapted to the r	0	
74LVC2G126_Q100 v.2	20161214	Product data sheet	-	74LVC2G126_Q100 v.1
Modifications:	• <u>Table 7</u> : The	e maximum limits for leaka	ge current and su	pply current have changed
74LVC2G126_Q100 v.1	20150512	Product data sheet	-	-

# 15. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <u>https://www.nexperia.com</u>.

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