

BUK9K12-60E

Dual N-channel 60 V, 11.5 mΩ logic level MOSFET

May 2014 Product data sheet

1. General description

Dual logic level N-channel MOSFET in an LFPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with V_{GS(th)} rating of greater than 0.5 V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	60	V
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; <u>Fig. 2</u>	[1]	-	-	35	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	68	W
Static characteristics FET1 and FET2							
R _{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ °C}; Fig. 11$		-	9.5	11.5	mΩ
Dynamic characteristics FET1 and FET2							
Q_{GD}	gate-drain charge	I _D = 15 A; V _{DS} = 48 V; V _{GS} = 5 V; T _j = 25 °C; <u>Fig. 13</u> ; <u>Fig. 14</u>		-	8.27	-	nC

[1] Continuous current is limited by package.



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	8 7 6 5	D1 D1 D2 D2
2	G1	gate1	1/	
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2	l î î î	mbk725
7	D1	drain1	1 2 3 4 LFPAK56D (SOT1205)	
8	D1	drain1	2	

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
BUK9K12-60E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205			

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K12-60E	91260E

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	60	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 k Ω		-	60	V
V_{GS}	gate-source voltage	T _j ≤ 175 °C; DC		-10	10	V
		T _j ≤ 175 °C; Pulsed	[1][2]	-15	15	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	68	W
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 5 V; <u>Fig. 2</u>	[3]	-	35	Α
		T _{mb} = 100 °C; V _{GS} = 5 V; <u>Fig. 2</u>	[3]	-	35	Α

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Symbol	Parameter	Conditions		Min	Max	Unit
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; Fig. 3	<u> </u>	-	204	Α
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-dra	in diode FET1 and FET2	'	'			
Is	source current	T _{mb} = 25 °C	[3]	-	35	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	204	Α
Avalanche	Ruggedness FET1 and FET2	'		'		
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 35 A; $V_{sup} \le 60 \text{ V}$; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; Fig. 4	[4][5]	-	118	mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T_i and or V_{GS}
- [3] Continuous current is limited by package.
- [4] Refer to application note AN10273 for further information
- [5] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

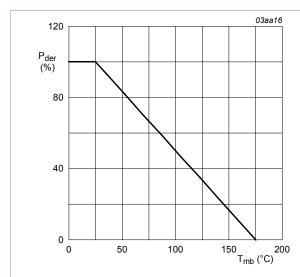


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

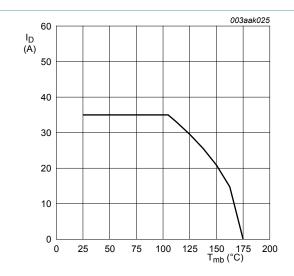


Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{\rm GS} \geq 5V$$

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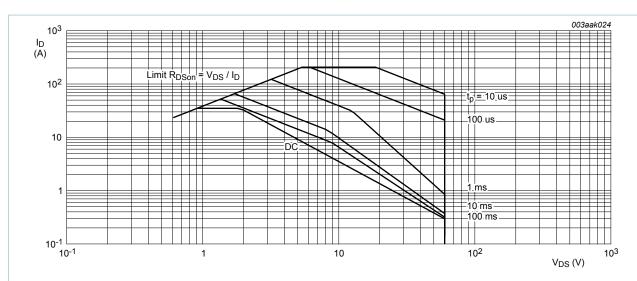
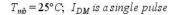


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



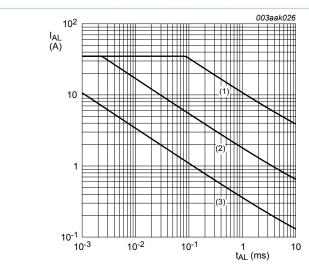


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j (int)} = 25^{\circ}C$; (2) $T_{j (int)} = 150^{\circ}C$; (3) Repetitive Avalanche

9. Thermal characteristics

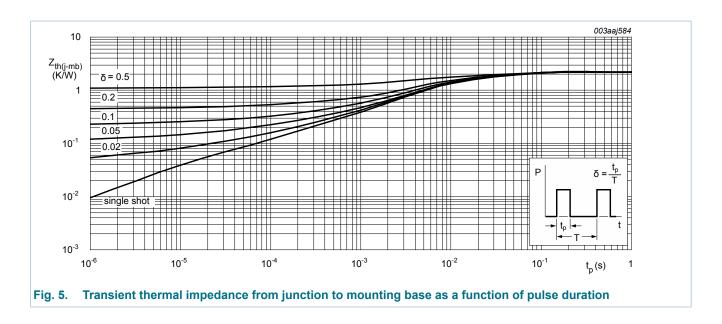
Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	-	2.21	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics FET1 and FET2				'	_
V _{(BR)DSS}	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	54	-	-	V
	breakdown voltage	$I_D = 250 \ \mu A; \ V_{GS} = 0 \ V; \ T_j = 25 \ ^{\circ}C$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C};$ Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 9; Fig. 10	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 9; Fig. 10	-	-	2.45	V
I _{DSS} drain	drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C	-	0.02	1	μΑ
		V _{DS} = 60 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μΑ
I _{GSS}	gate leakage current	V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state	V _{GS} = 5 V; I _D = 15 A; T _j = 25 °C; <u>Fig. 11</u>	-	9.5	11.5	mΩ
	resistance	V _{GS} = 5 V; I _D = 15 A; T _j = 175 °C; Fig. 11; Fig. 12	-	21.5	26	mΩ
		V_{GS} = 10 V; I_{D} = 15 A; T_{j} = 25 °C; Fig. 11	-	8.5	10.7	mΩ
Dynamic ch	naracteristics FET1 and FE	ET2	'			,
Q _{G(tot)}	total gate charge	I _D = 15 A; V _{DS} = 48 V; V _{GS} = 5 V;	-	24.5	-	nC
Q _{GS}	gate-source charge	T _j = 25 °C; <u>Fig. 13; Fig. 14</u>	-	5.4	-	nC

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Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Q_{GD}	gate-drain charge			-	8.27	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz;		-	2602	3470	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 15</u>		-	237	284	pF
C _{rss}	reverse transfer capacitance			-	126	173	pF
t _{d(on)}	turn-on delay time	V_{DS} = 48 V; R_L = 3.2 Ω ; V_{GS} = 5 V; $R_{G(ext)}$ = 5 Ω ; T_j = 25 °C; I_D = 15 A		-	15.1	-	ns
t _r	rise time			-	28	-	ns
t _{d(off)}	turn-off delay time			-	31.5	-	ns
t _f	fall time	_		-	25.3	-	ns
Source-dra	in diode FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 10 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 ^{\circ}\text{C}$; Fig. 16		-	0.78	1.2	V
t _{rr}	reverse recovery time	$I_S = 15 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$		-	22.6	-	ns
Q _r	recovered charge	$V_{DS} = 30 \text{ V}; T_j = 25 \text{ °C}$		-	18.1	-	nC

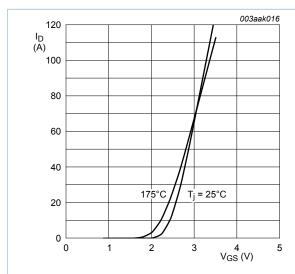


Fig. 6. Transfer characteristics; drain current as a function of gate-source voltage; typical values



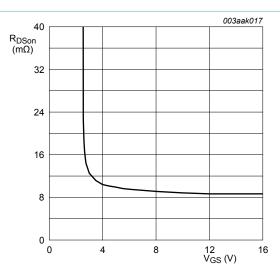


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^{\circ}C; \ I_D = 15A$$

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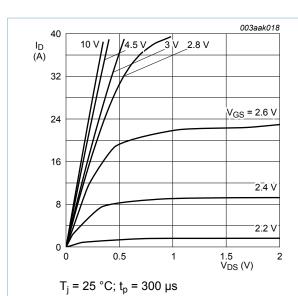


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

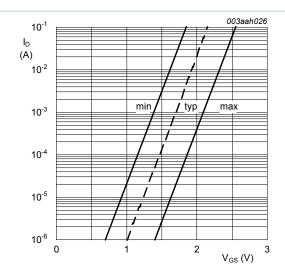


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25$$
°C; $V_{DS} = 5V$

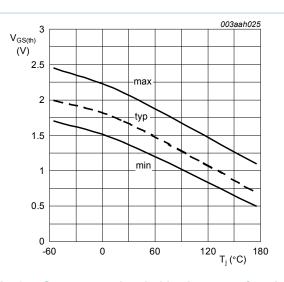
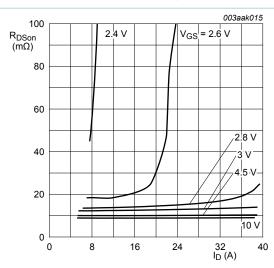


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1 \text{ mA}; \ V_{DS} = V_{GS}$$



 $T_i = 25 \, ^{\circ}\text{C}; t_p = 300 \, \mu\text{s}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

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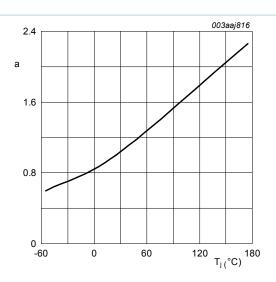


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon (25^{\circ}C)}}$$

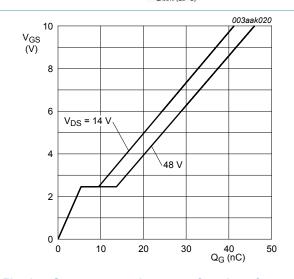


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25$$
°C; $I_D = 15A$

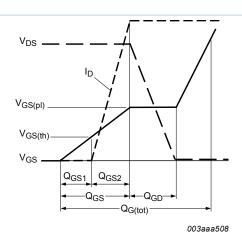


Fig. 13. Gate charge waveform definitions

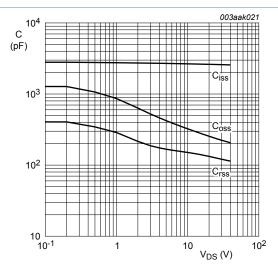


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = \mathbf{0}V; \ f = \mathbf{1}MHz$$

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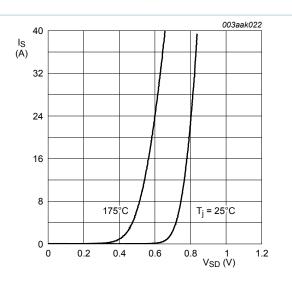


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

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11. Package outline

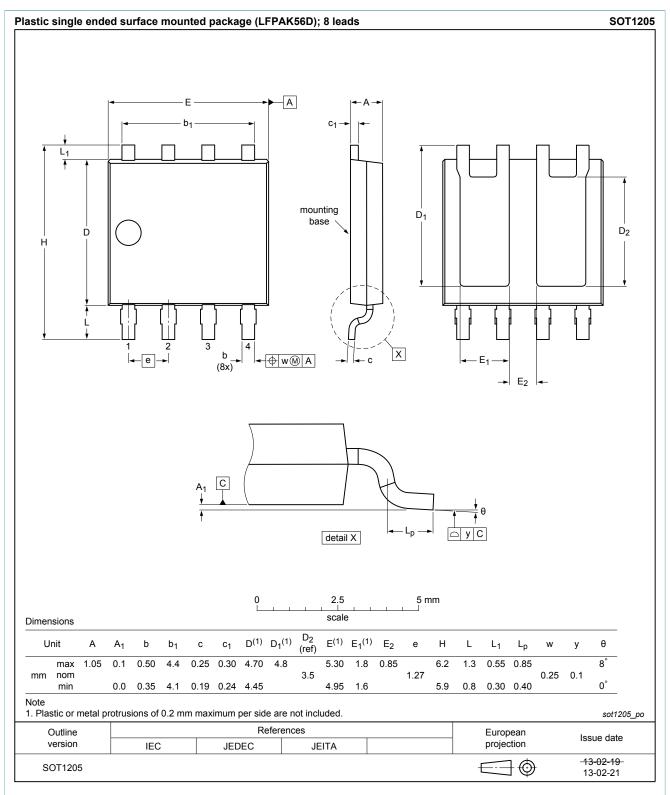


Fig. 17. Package outline LFPAK56D (SOT1205)

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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