

MMBZ33VBU-Q

Low capacitance bidirectional dual line ESD protection diode 4 April 2024 Product data sheet

1. General description

ESD protection device in a small SOT323 (SC-70) Surface-Mounted Device (SMD) plastic package, designed to protect two lines from the damage caused by ElectroStatic Discharge (ESD) and other transients.

2. Features and benefits

- Reverse stand-off voltage: V_{RWM} = 27 V
- Low clamping voltage: V_{CL} = 31 V at I_{PP} = 3.9 A
- ESD protection up to 30 kV (IEC 61000-4-2)
- Low capacitance: C_d = 9 pF
- High temperature capability: T_i = 175 °C
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- Automotive electronic control units
- Portable electronics

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Мах	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	27	V
I _{PPM}	rated peak pulse current	t _p = 8/20 μs	[1] [2]	-	-	3.9	A
V _{CL}	clamping voltage	I_{PPM} = 3.9 A; t _p = 8/20 µs; T _{amb} = 25 °C	[2] [3]	-	31	42	V

[1] According to IEC 61000-4-5

[2] Measured from pin 1 or 2 to pin 3

[3] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5

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5. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	3	
2	K2	cathode (diode 2)		
3	CC	common cathode	1 2 SC-70 (SOT323)	K1 CC K2 CC 006aaa155

6. Ordering information

Table 3. Ordering information

Type number	Package	ackage				
	Name	Description	Version			
MMBZ33VBU-Q	SC-70	plastic, surface-mounted package; 3 leads; 1.3 mm pitch; 2 mm x 1.25 mm x 0.95 mm body	SOT323			

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
MMBZ33VBU-Q	Q3%

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

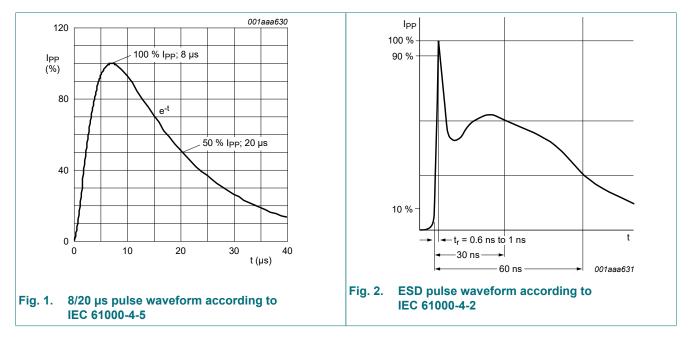
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I _{PPM}	rated peak pulse current	t _p = 8/20 μs	[1] [2]	-	3.9	А
Tj	junction temperature			-	175	°C
T _{amb}	ambient temperature			-55	175	°C
T _{stg}	storage temperature			-65	175	°C
ESD maximu	m ratings		•			
V _{ESD}	electrostatic discharge	IEC 61000-4-2 (contact discharge)	[2] [3]	-	30	kV
	voltage	ISO10605; contact discharge; C = 330 pF, R = 330 Ω	[2] [3]	-	30	kV
		ISO10605; contact discharge; C = 150 pF, R = 330Ω	[2] [3]	-	30	kV

[1] According to IEC 61000-4-5

[2] Measured from pin 1 or 2 to pin 3

[3] Device stressed with ten non-repetitive ESD pulses



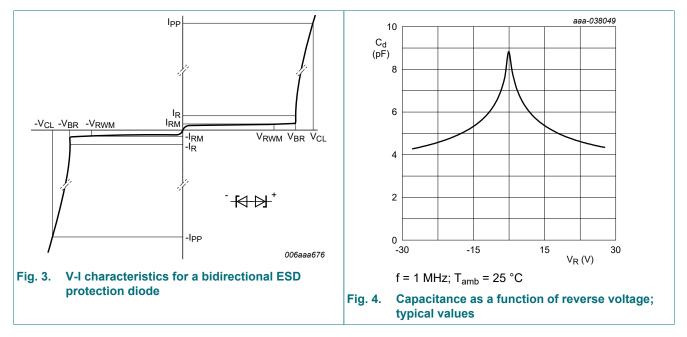
9. Characteristics

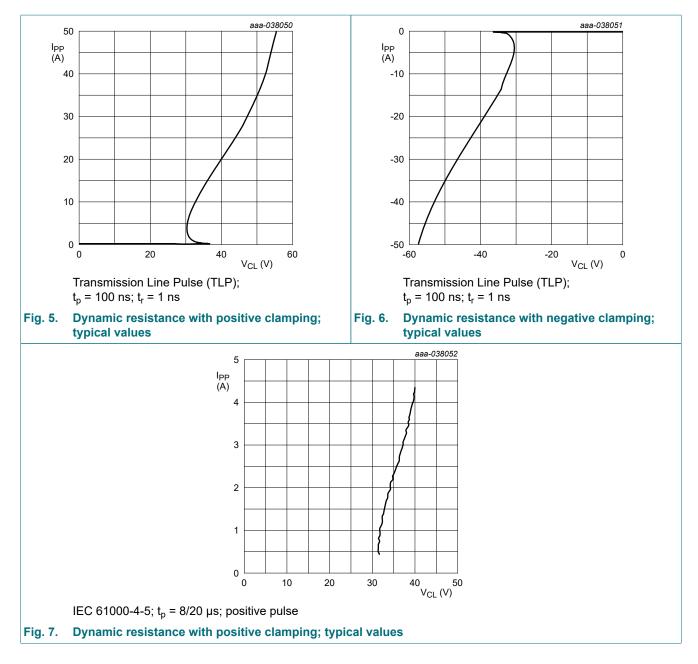
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	27	V
V _{BR}	breakdown voltage	I _R = 10 mA; T _{amb} = 25 °C	[1]	28	33	38	V
I _{RM}	reverse leakage current	V _{RWM} = 27 V; T _{amb} = 25 °C	[1]	-	1	50	nA
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C	[1]	-	9	10	pF
V _{CL}	clamping voltage	I _{PPM} = 3.9 A; t _p = 8/20 μs; T _{amb} = 25 °C	[1] [2]	-	31	42	V
		I _{PP} = 16 A; t _p = 100 ns; T _{amb} = 25 °C	[1] [3]	-	37	-	V

Measured from pin 1 or 2 to pin 3 [1]

[2]

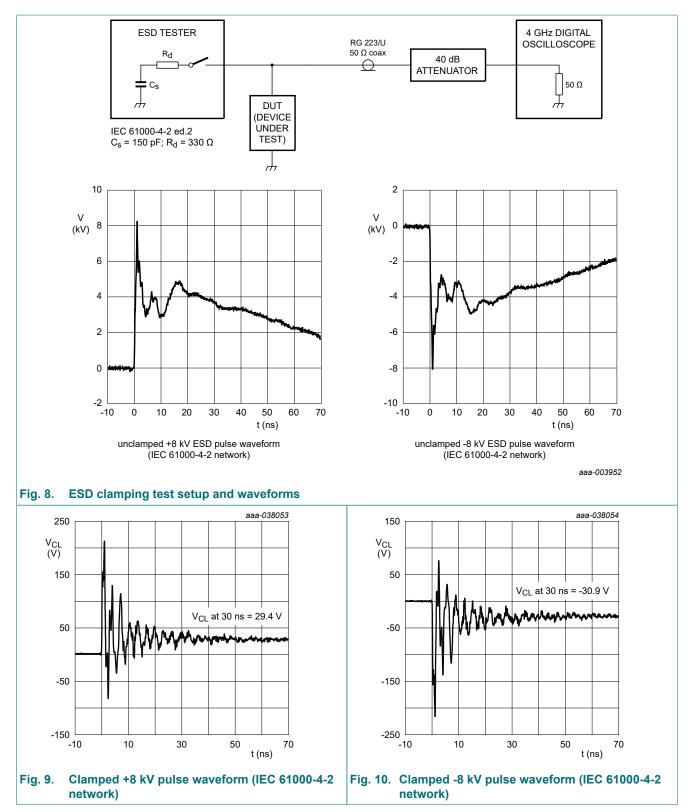
Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5 Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008 [3]





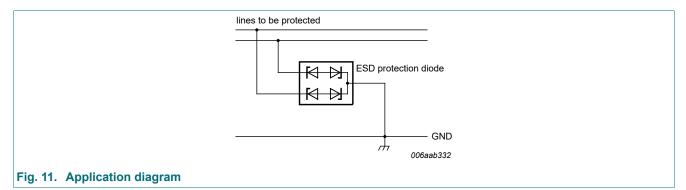
MMBZ33VBU-Q

Low capacitance bidirectional dual line ESD protection diode



10. Application information

The device is designed for the protection of two lines from the damage caused by ESD and surge pulses.



Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

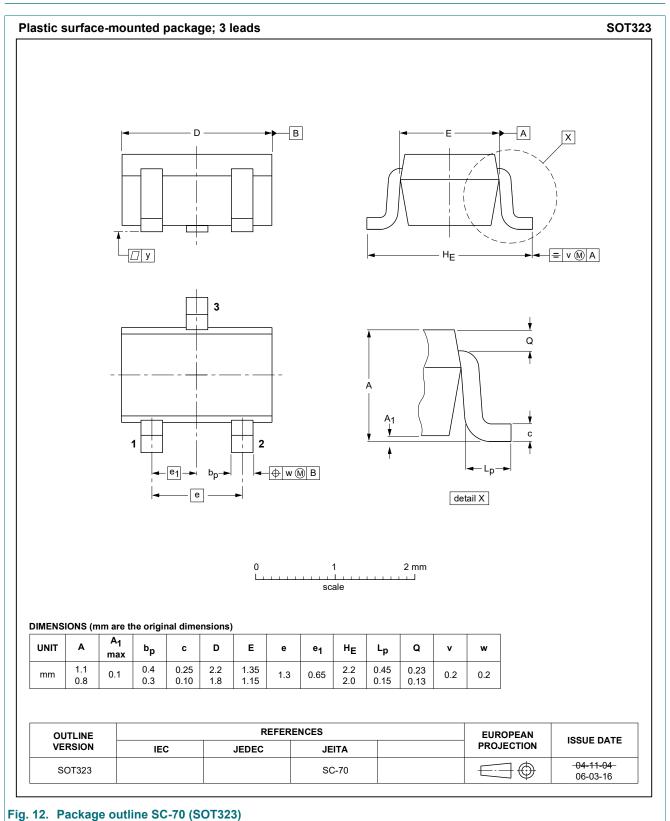
- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

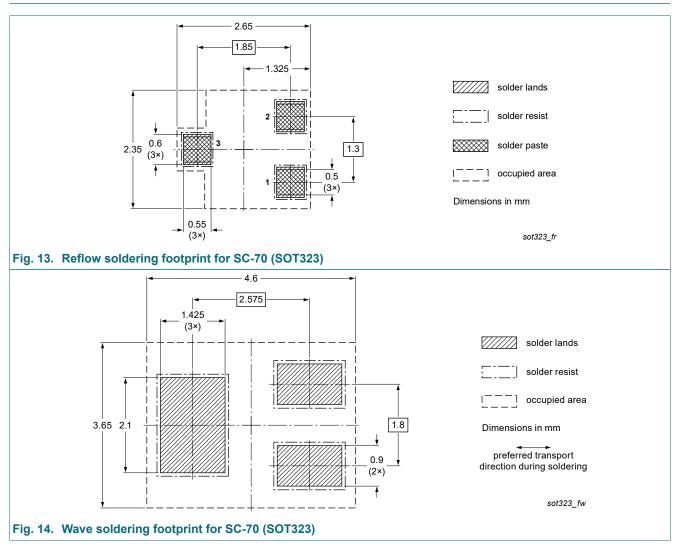
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline



13. Soldering



14. Revision history

Table 7. Revision history					
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes	
MMBZ33VBU-Q v.1	20240404	Product data sheet	-	-	

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <u>https://www.nexperia.com</u>.

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