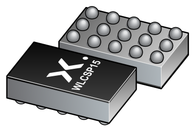


NEX10001UB

220 mA dual output LCD bias power supply

Rev. 2 — 20 December 2023 Product data sheet

1. General description

The NEX10001 is a power supply IC providing programmable positive and negative output voltages for TFT-LCD panels. The device features an integrated boost converter, LDO regulator and a negative charge pump. The device requires only a single inductor allowing for a small Bill-Of-Material and the smallest PCB area.

The NEX10001 has an input voltage range of 2.7 V to 5 V and can operate from single-cell Li-ion, Ni-Li and Li-Polymer batteries It can supply up to 220 mA output current. The NEX10001 has excellent line transient and load transient responses.

2. Features and benefits

- Input voltage range: 2.7 V to 5 V
- Programmable output voltages:
  - OUTP: +4 V to +6.5 V (0.1 V step)
  - OUTN: -4 V to -6.5 V (0.1 V step)
- Maximum output current: 220 mA
- 85% high efficiency at 80 mA combined output
- ±1% output voltage accuracy
- Excellent transient response
- I²C Interface:
  - Flexible output voltage programming
- Integrated active output discharge function
- UVLO and OTSD protection
- Wafer level chip-scale package; 15 bumps; 1.16 × 1.96 × 0.62 mm body (0.4 mm pitch)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C2a exceeds 500 V
- Specified from -40 °C to +85 °C

3. Applications

- Smart phone TFT-LCD
- Tablet TFT-LCD

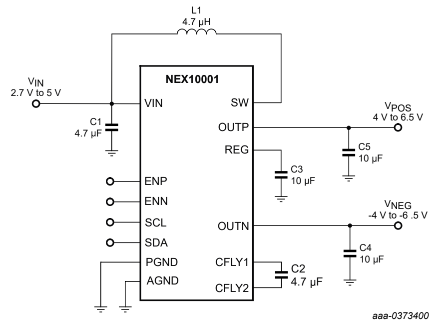
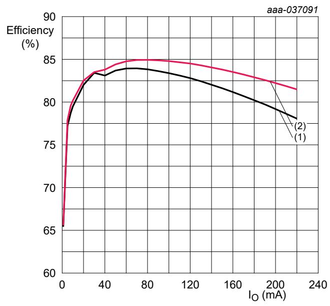


Fig. 1. Typical application



V_{POS} = 5.4 V; V_{NEG} = -5.4 V

(1) V_{IN} = 3.7 V

(2) V_{IN} = 4.5 V

Fig. 2. Efficiency versus output current (I_O)

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NEX10001UB	-40 °C to +85 °C	WLCSP15	wafer level chip-scale package; 15 bumps; 1.16 × 1.96 × 0.62 mm body	SOT8054-1

5. Marking

Table 2. Marking codes

Type number	Marking code
NEX10001UB	NX01A

6. Functional diagram

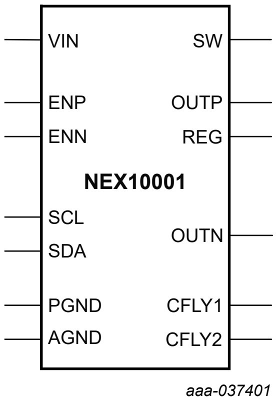
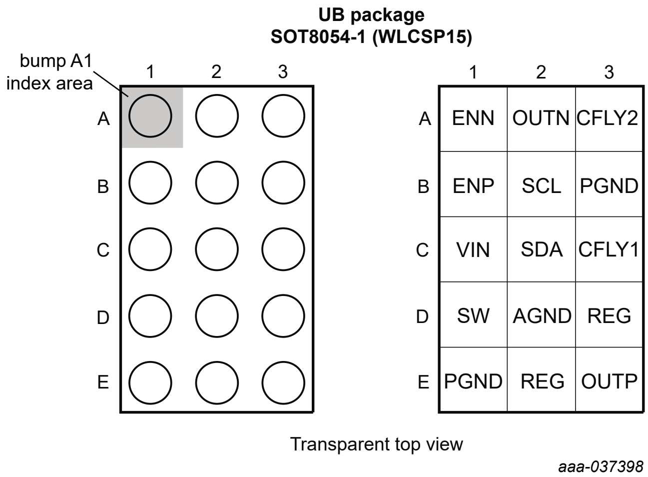


Fig. 3. Logic symbol

7. Pinning information

7.1. Pinning



Solder bump facing down

Fig. 4. Bump configuration SOT8054-1 (WLCSP15)

7.2. Pin description

Table 3. Pin description

Symbol	Bump	I/O	Description
	WLCSP15		
ENN	A1	I	Enable pin for V_{NEG} rail
OUTN	A2	O	Output pin of the negative charge pump (V_{NEG})
CFLY2	A3	I/O	Negative charge pump flying capacitor pin
ENP	B1	I	Enable pin for V_{POS} rail
SCL	B2	I/O	I²C interface clock signal pin
PGND	B3	-	Power ground
VIN	C1	I	Input voltage supply pin
SDA	C2	I/O	I²C interface data signal pin
CFLY1	C3	I/O	Negative charge pump flying capacitor pin
SW	D1	I/O	Switch pin of the boost converter
AGND	D2	-	Analog ground
REG	D3	I/O	Boost converter output pin
PGND	E1	-	Power ground
REG	E2	I/O	Boost converter output pin
OUTP	E3	O	Output pin of the LDO (V_{POS})

8. Device comparison

Table 4. Device Comparison

Type number	Output current (I_{OUT})
NEX10001UB	220 mA
NEX10000UB[1]	80 mA

[1] Please see detail parameters from NEX10000UB data sheet.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	pins ENN, ENP, VIN	-0.3	+5.5	V
V_O	output voltage	pin OUTN	-7	+0.3	V
		pin OUTP	-0.3	+7.0	V
V_{IO}	input/output voltage	pins SCL, SDA	-0.3	+5.5	V
		pins CFLY1, REG	-0.3	+7.1	V
		pin SW	-0.3	+7.5	V
		pin CFLY2	-7	+0.3	V
T_j	junction temperature		-40	+150	°C
T_{amb}	ambient temperature		-40	+85	°C
T_{stg}	storage temperature		-65	+150	°C
ESD ratings					
V_{ESD}	electrostatic discharge	HBM: ANSI/ESDA/JEDEC JS-001 class 2	-	±2000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C2a	-	±500	V

10. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	input voltage	supply voltage pin VIN	2.7	-	5.0	V
I_O	output current	[1]	-	-	220	mA
L	inductor		2.2	-	4.7	µH
C_O	output capacitance	pins OUTN, OUTP, REG	4.7	10	-	µF
C_{IO}	input/output capacitance	pins CFLY1, CFLY2	2.2	-	4.7	µF
C_I	input capacitance	pin VIN	-	4.7	-	µF
T_{amb}	ambient temperature		-40	-	+85	°C
T_j	junction temperature		-40	-	+125	°C

[1] to support $I_{POS} + I_{NEG} > 360$ mA, $V_{IN} \geq 3$ V is required.

11. Thermal Information

Table 7. Thermal information

Symbol	Parameter	Package	Unit
		SOT8054-1 (WLCSP15)	
$R_{θJA}$	Junction to ambient thermal resistance	76.4[1]	°C/W

[1] Measured in still air-free convection condition (conforms to EIA/JESD51-2) on high effective thermal conductivity JESD51-9 with a test board PCB.

12. Electrical characteristics

Table 8. Electrical characteristics

At recommended operating conditions; V_{IN} = 3.7 V; V_{ENN} = V_{ENP} = V_{IN}; V_{POS} = 5.4 V; V_{NEG} = –5.4 V; (unless otherwise noted) voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
Supply						
V_{IN}	input voltage range		2.7	-	5.0	V
V_{UVLO}	undervoltage lockout threshold	V_{IN} rising	2.35	2.4	2.5	V
		V_{IN} falling	2.1	2.2	2.25	V
I_q	quiescent current	V_{ENP} = V_{ENN} = 3.7 V, switching	-	0.79	1.04	mA
I_{sd}	shutdown current	V_{ENP} = V_{ENN} = 0 V, no switching	-	-	1	μA
T_{sd}	shutdown temperature	[2]	-	140	-	°C
$T_{sd(hys)}$	shutdown temperature hysteresis	[2]	-	30	-	°C
Logic ENN, ENP						
V_{IH}	HIGH-level input voltage	V_{IN} = 2.7 V to 5 V	1.27	-	-	V
V_{IL}	LOW-level input voltage	V_{IN} = 2.7 V to 5 V	-	-	0.53	V
R_{EN}	pull-down resistor		-	220	-	KΩ
Logic SCL, SDA						
V_{IH}	HIGH-level input voltage	V_{IN} = 2.7 V to 5 V	1.27	-	-	V
V_{IL}	LOW-level input voltage	V_{IN} = 2.7 V to 5 V	-	-	0.53	V
Boost Converter						
I_{LIM}	boost converter current limit		1.3	1.6	1.9	A
f_{SW}	switching frequency	Boost converter switching frequency	1.15	1.4	1.65	MHz

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
LDO output V_{POS}						
V_{POS}	positive output voltage range		4.0	-	6.5	V
V_{POS_acc}	positive output voltage accuracy		-1%	-	1%	
I_{POS}	positive output current capability		220	-	-	mA
I_{POS_lim}	positive output current limit	Register 0x02 LDO_CL = 0	255	275	310	mA
		Register 0x02 LDO_CL = 1	-	370	-	mA
V_{DROP}	dropout voltage	V_{REG} = $V_{POS(nom)}$ = 5.4 V, I_{OUT} = 80 mA	-	66	-	mV
		V_{REG} = $V_{POS(nom)}$ = 5.4 V, I_{OUT} = 220 mA	-	192	-	mV
ΔV_{LR}	line regulation	V_{IN} = 2.7 V to 5 V, I_{OUT} = 220 mA [2]	-	5	-	mV
ΔV_{LDR}	load regulation	V_{IN} = 3.7 V, ΔI_{OUT} = 220 mA [2]	-	15	-	mV
R_D	discharge resistor		-	23	-	Ω
Negative charge pump output V_{NEG}						
V_{NEG}	negative output voltage range		-6.5	-	-4.0	V
V_{NEG_acc}	negative output voltage accuracy		-1%	-	1%	V
I_{NEG}	negative output current capability		220	-	-	mA
I_{NEG_lim}	negative output current limit		245	275	310	mA
f_{OSC}	negative charge pump switching frequency		0.85	1	1.15	MHz
ΔV_{LR}	line regulation	V_{IN} = 2.7 V to 5 V, I_{OUT} = 220 mA [2]	-	5	-	mV
ΔV_{LDR}	load regulation	V_{IN} = 3.7 V, ΔI_{OUT} = 220 mA [2]	-	10	-	mV
R_D	discharge resistor		-	17.5	-	Ω
I²C Interface						
V_{IH}	HIGH-level input voltage	SDA, SCL, 2.7 V ≤ V_{IN} ≤ 5.0 V	1.27	-	-	V
V_{IL}	LOW-level input voltage	SDA, SCL, 2.7 V ≤ V_{IN} ≤ 5.0 V	-	-	0.53	V
f_{SCL}	SCL clock frequency	pin SCL	-	-	400	KHz

[1] All typical values are measured at T_{amb} = 25 °C.
[2] Guaranteed by bench test, not fully tested in production.

13. Typical characteristics

Table 9. Component list for typical characteristics circuit

V_{IN} = V_{ENN} = V_{ENP} = 3.7 V; V_{POS} = 5.4 V; V_{NEG} = –5.4 V; T_{amb} = 25 °C; unless otherwise noted; voltages are referenced to GND (ground = 0 V). See Fig. 5

Components	Description	Manufacture and part number
C1	4.7 µF, 10 V, 0603, X5R, ceramic	TDK-C1608X5R1E475K080AC
C2	4.7 µF, 16 V, 0603, X5R, ceramic	TDK-C1608X5R1C225KTK00E
C3, C4, C5	10 µF, 10 V, 0603, X5R, ceramic	TDK-C1608X5R1E106K080AC
L1	4.7 µF, 2.2 A, 180 mΩ, 2.5 mm × 2.0 mm × 1.2 mm	TDK-TMS252012ALM-4R7MTAA
U1	NEX10001UB	NEXPERIA

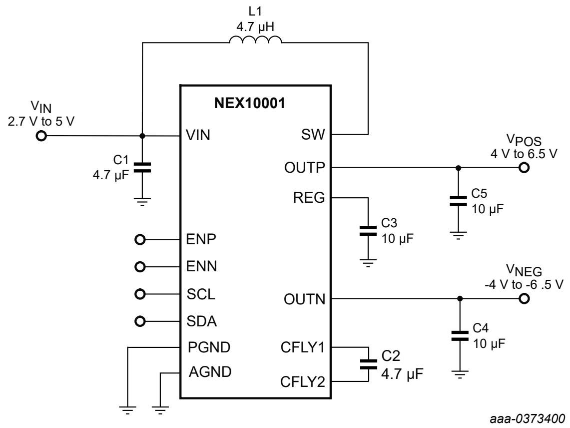
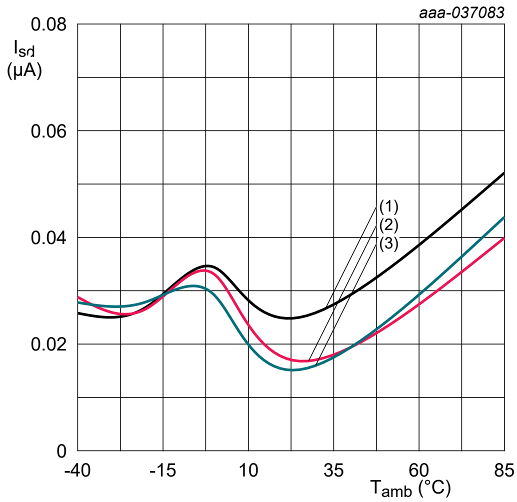
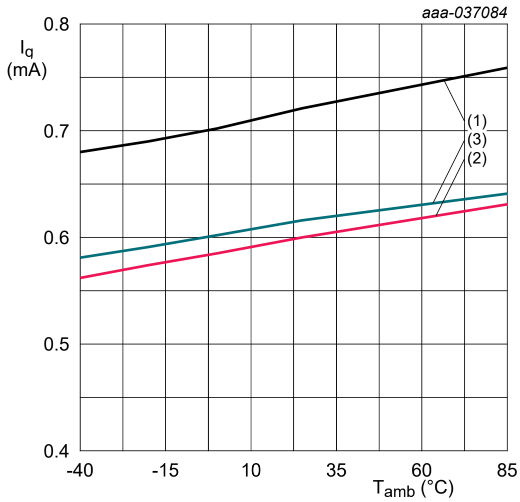


Fig. 5. Typical application



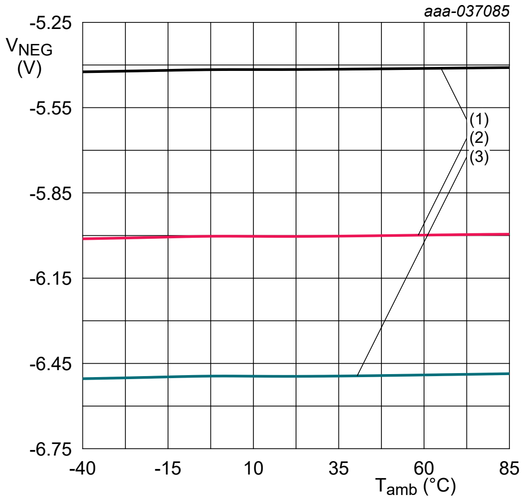
(1) V_{IN} = 2.7 V
(2) V_{IN} = 3.7 V
(3) V_{IN} = 4.5 V

Fig. 6. Shutdown current (I_{sd}) versus ambient temperature (T_{amb})



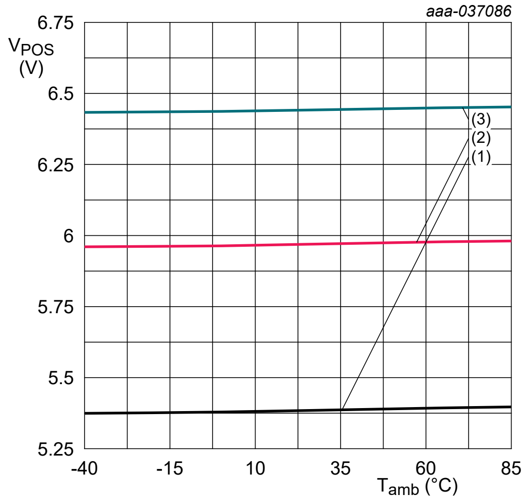
(1) V_{IN} = 2.7 V
(2) V_{IN} = 3.7 V
(3) V_{IN} = 4.5 V

Fig. 7. Quiescent current (I_q) versus ambient temperature (T_{amb})



(1) V_{NEG} = -5.4 V
(2) V_{NEG} = -6 V
(3) V_{NEG} = -6.5 V

Fig. 8. Negative output voltage (V_{NEG}) versus ambient temperature (T_{amb})



(1) V_{POS} = 5.4 V
(2) V_{POS} = 6 V
(3) V_{POS} = 6.5 V

Fig. 9. Positive output voltage (V_{POS}) versus ambient temperature (T_{amb})

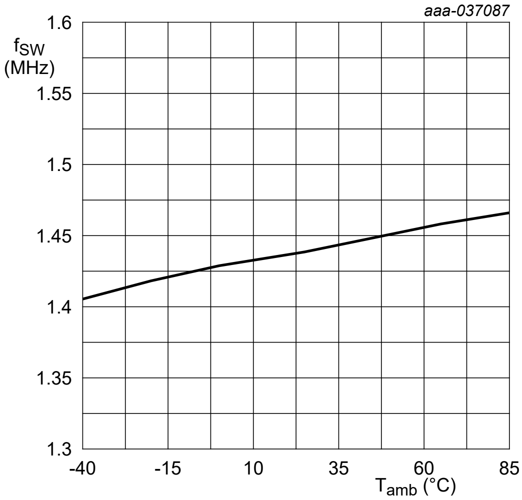
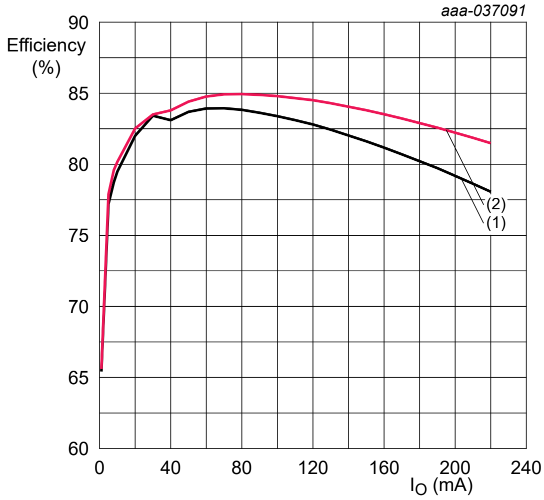
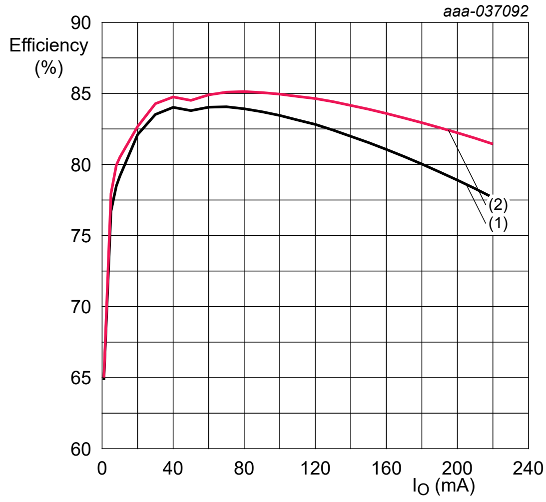


Fig. 10. Boost converter switching frequency (f_{SW}) versus ambient temperature (T_{amb})



V_{POS} = 5.4 V; V_{NEG} = -5.4 V
(1) V_{IN} = 3.7 V
(2) V_{IN} = 4.5 V

Fig. 11. Efficiency versus output current (I_O)

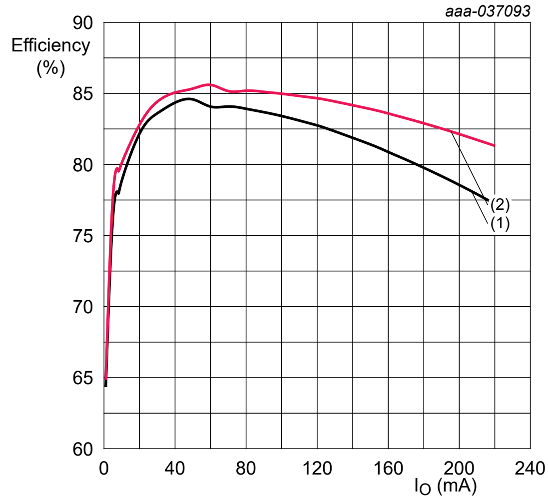


V_{POS} = 6 V; V_{NEG} = -6 V

(1) V_{IN} = 3.7 V

(2) V_{IN} = 4.5 V

Fig. 12. Efficiency versus output current (I_O)

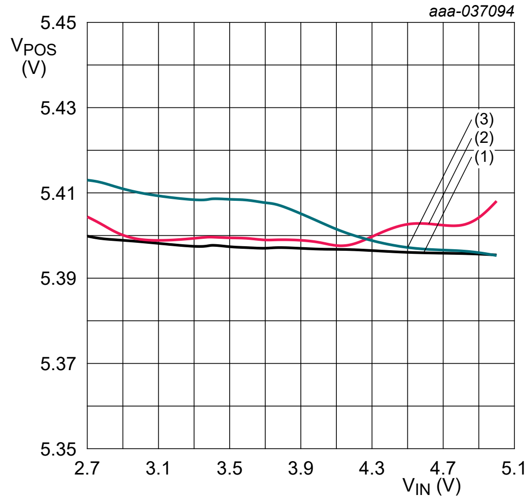


V_{POS} = 6.5 V; V_{NEG} = -6.5 V

(1) V_{IN} = 3.7 V

(2) V_{IN} = 4.5 V

Fig. 13. Efficiency versus output current (I_O)



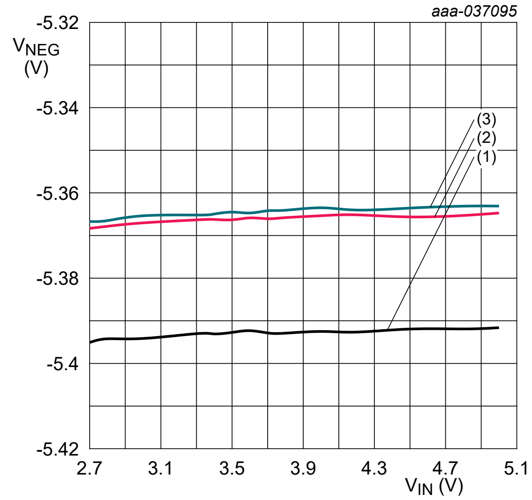
V_{POS} = 5.4 V

(1) I_{POS} = 0 mA

(2) I_{POS} = 80 mA

(3) I_{POS} = 200 mA

Fig. 14. V_{POS} versus V_{IN} line regulation



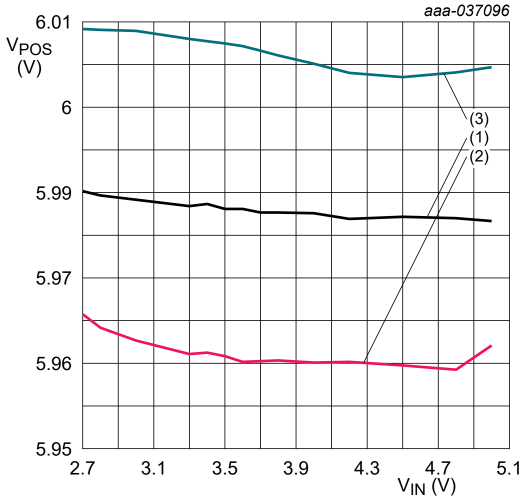
V_{NEG} = -5.4 V

(1) I_{NEG} = 0 mA

(2) I_{NEG} = 80 mA

(3) I_{NEG} = 200 mA

Fig. 15. V_{NEG} versus V_{IN} line regulation



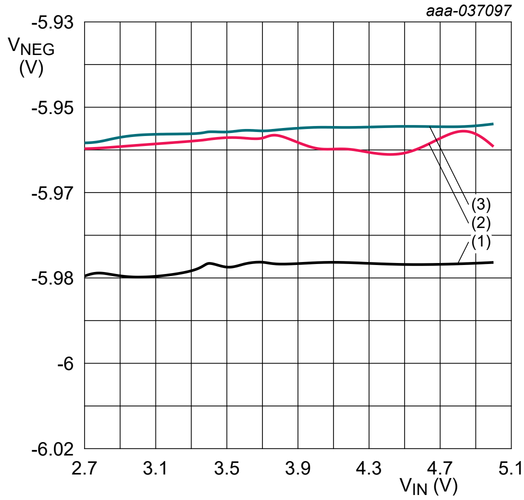
V_{POS} = 6 V

(1) I_{POS} = 0 mA

(2) I_{POS} = 80 mA

(3) I_{POS} = 200 mA

Fig. 16. V_{POS} versus V_{IN} line regulation



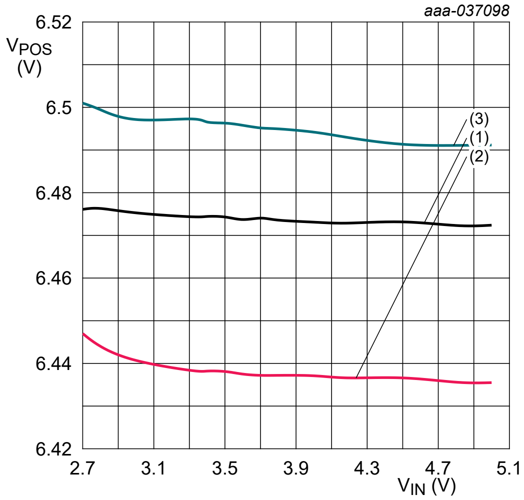
V_{NEG} = -6 V

(1) I_{NEG} = 0 mA

(2) I_{NEG} = 80 mA

(3) I_{NEG} = 200 mA

Fig. 17. V_{NEG} versus V_{IN} line regulation



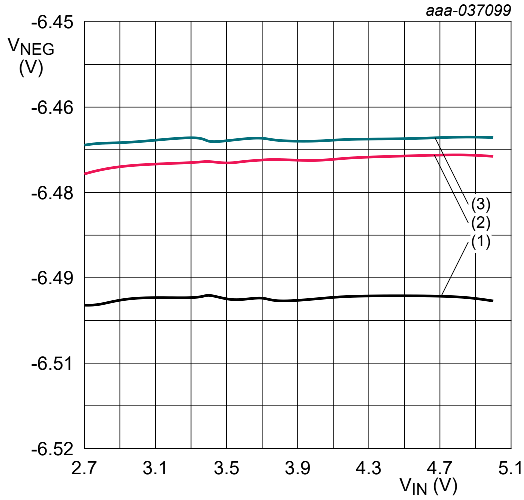
V_{POS} = 6.5 V

(1) I_{POS} = 0 mA

(2) I_{POS} = 80 mA

(3) I_{POS} = 200 mA

Fig. 18. V_{POS} versus V_{IN} line regulation



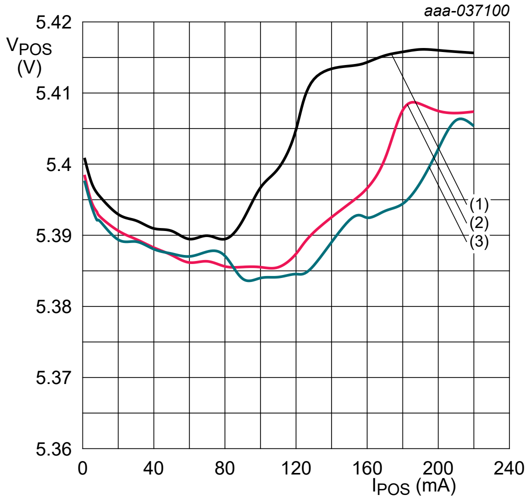
V_{NEG} = -6.5 V

(1) I_{NEG} = 0 mA

(2) I_{NEG} = 80 mA

(3) I_{NEG} = 200 mA

Fig. 19. V_{NEG} versus V_{IN} line regulation



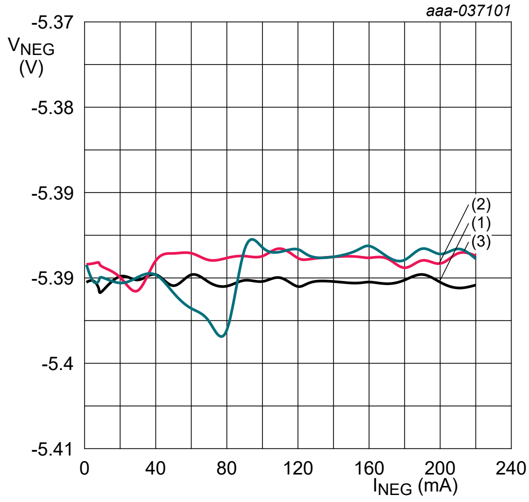
V_{POS} = 5.4 V

(1) V_{IN} = 2.7 V

(2) V_{IN} = 3.7 V

(3) V_{IN} = 4.5 V

Fig. 20. V_{POS} versus positive output current (load regulation)



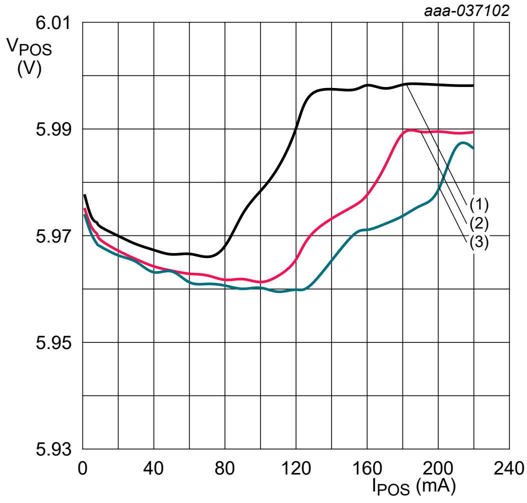
V_{NEG} = -5.4 V

(1) V_{IN} = 2.7 V

(2) V_{IN} = 3.7 V

(3) V_{IN} = 4.5 V

Fig. 21. V_{NEG} versus negative output current (load regulation)



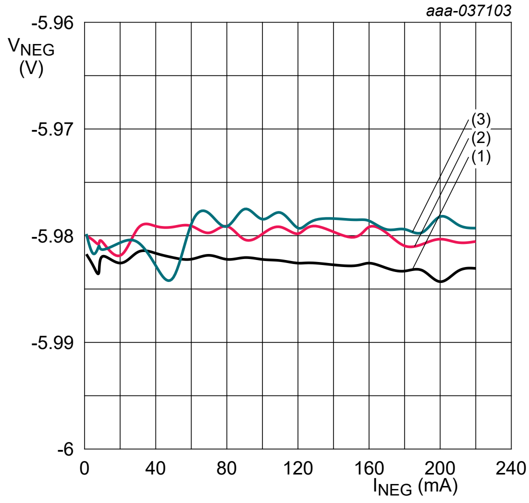
V_{POS} = 6 V

(1) V_{IN} = 2.7 V

(2) V_{IN} = 3.7 V

(3) V_{IN} = 4.5 V

Fig. 22. V_{POS} versus positive output current (load regulation)



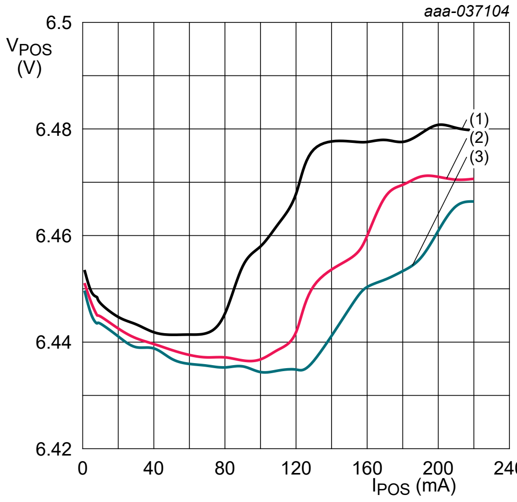
V_{NEG} = -6 V

(1) V_{IN} = 2.7 V

(2) V_{IN} = 3.7 V

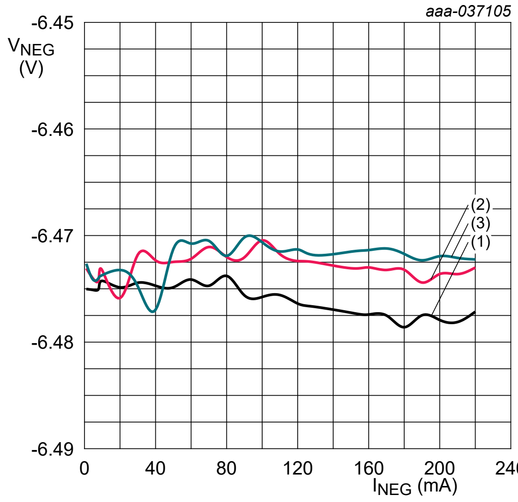
(3) V_{IN} = 4.5 V

Fig. 23. V_{NEG} versus negative output current (load regulation)



V_{POS} = 6.5 V
(1) V_{IN} = 2.7 V
(2) V_{IN} = 3.7 V
(3) V_{IN} = 4.5 V

Fig. 24. V_{POS} versus positive output current (load regulation)



V_{NEG} = -6.5 V
(1) V_{IN} = 2.7 V
(2) V_{IN} = 3.7 V
(3) V_{IN} = 4.5 V

Fig. 25. V_{NEG} versus negative output current (load regulation)

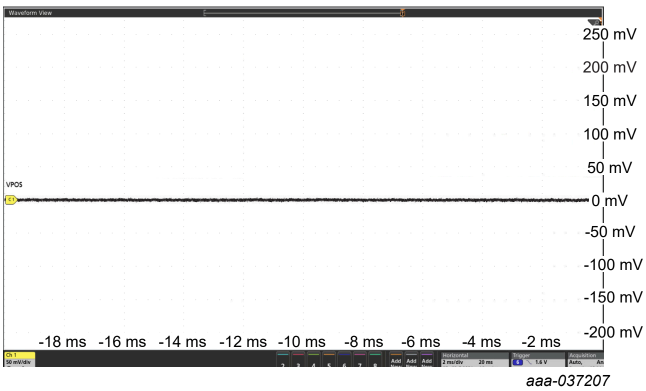


Fig. 26. V_{POS} output ripple (I_{POS} = 0 mA)

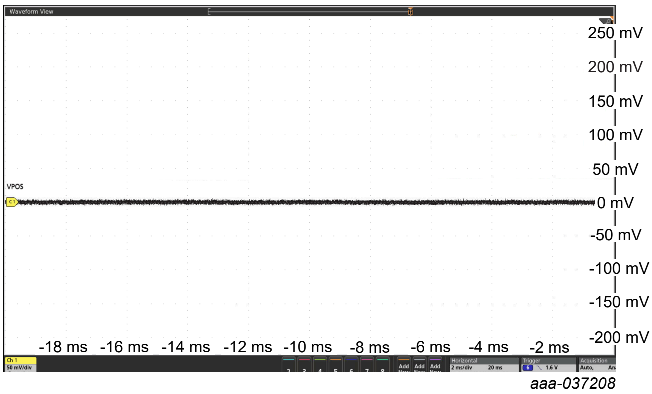


Fig. 27. V_{POS} output ripple (I_{POS} = 80 mA)

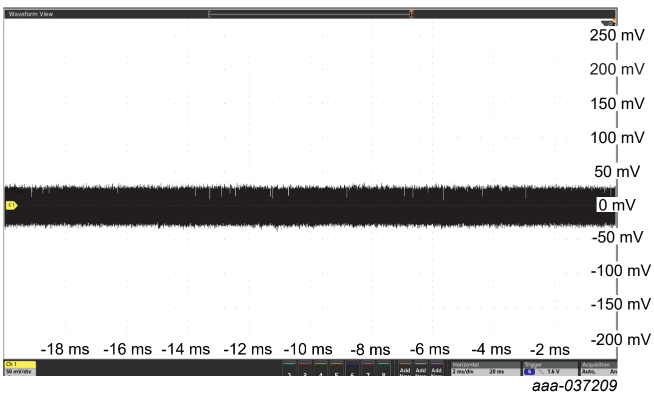


Fig. 28. V_{POS} output ripple (I_{POS} = 220 mA)

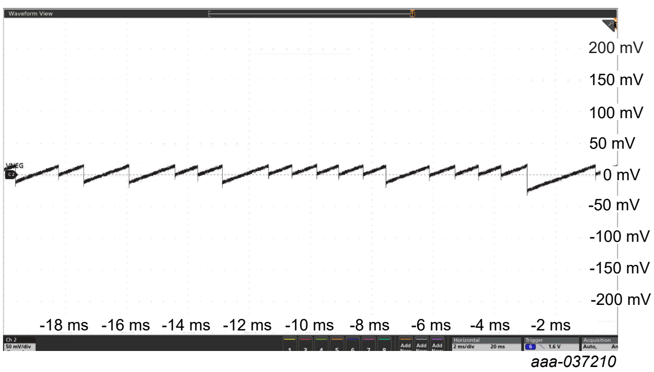


Fig. 29. V_{NEG} output ripple (I_{NEG} = 0 mA)

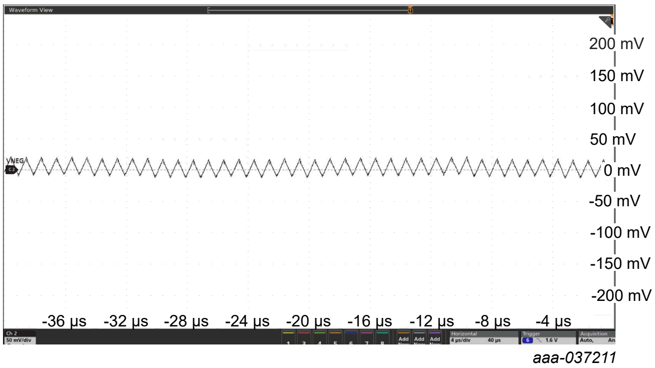


Fig. 30. V_{NEG} output ripple (I_{NEG} = 80 mA)

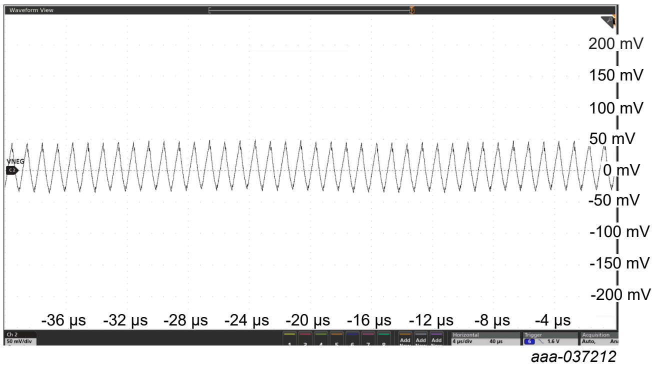


Fig. 31. V_{NEG} output ripple (I_{NEG} = 220 mA)

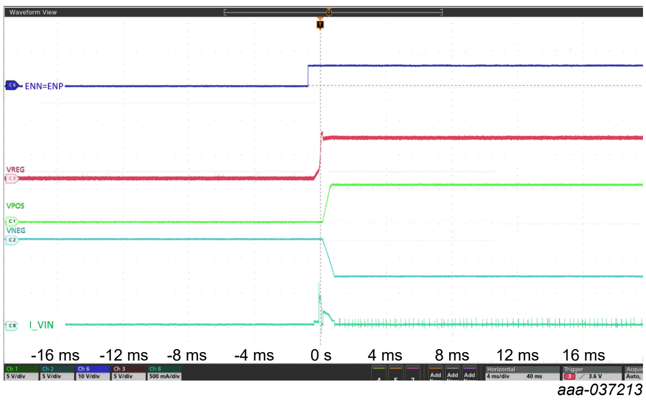


Fig. 32. Simultaneous power-up and inrush current

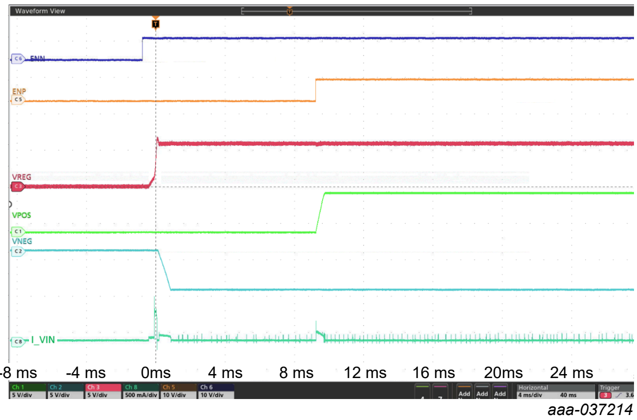


Fig. 33. Sequential power-up and inrush current

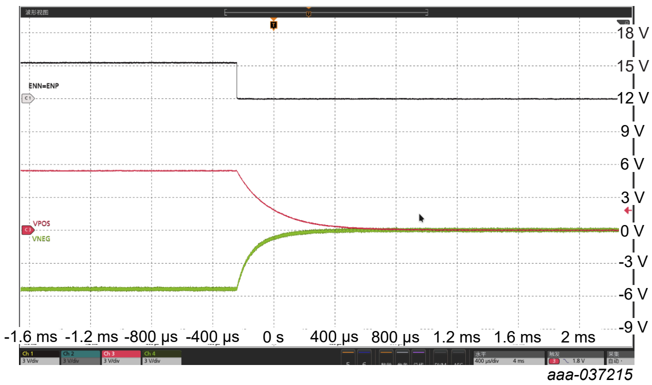


Fig. 34. Simultaneous shut-down

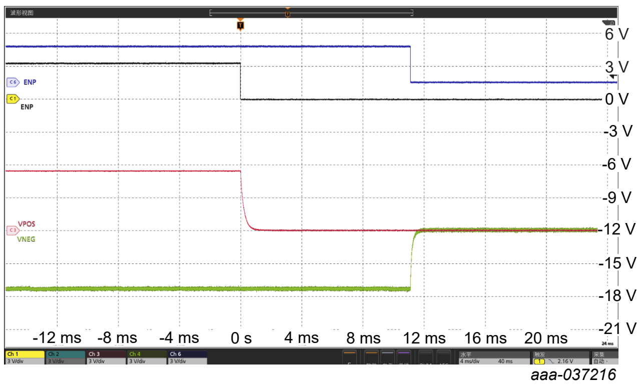
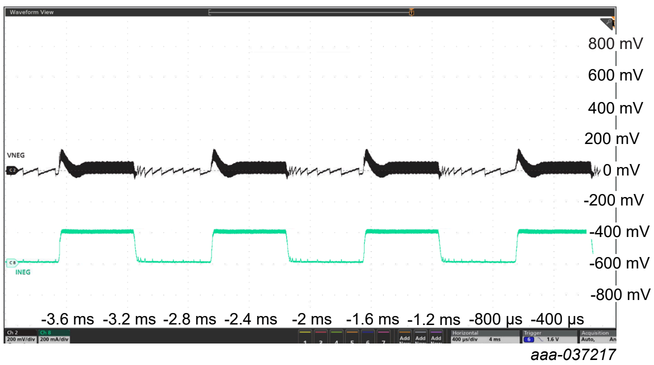
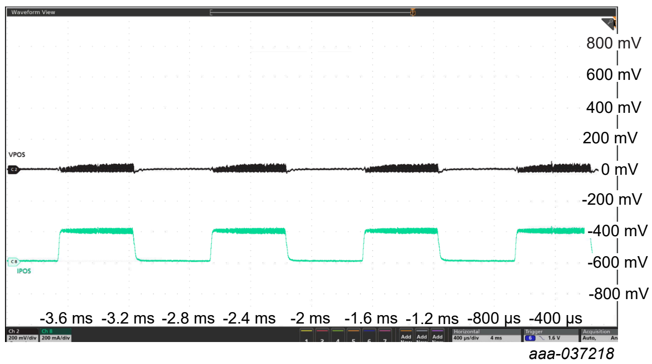


Fig. 35. Sequential shut-down



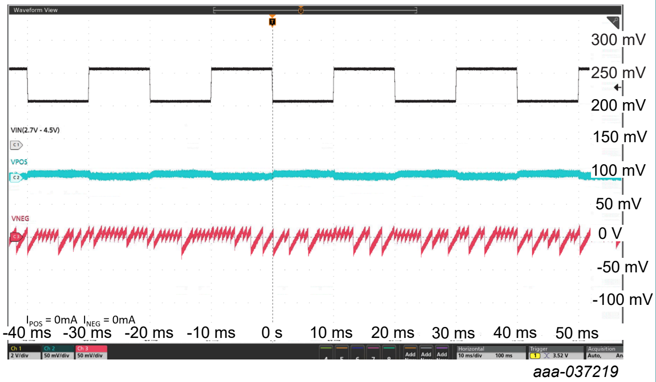
V_{NEG} = -5.4 V; I_{NEG} = 0 mA to 200 mA

Fig. 36. Load transient



V_{POS} = 5.4 V; I_{POS} = 0 mA to 200 mA

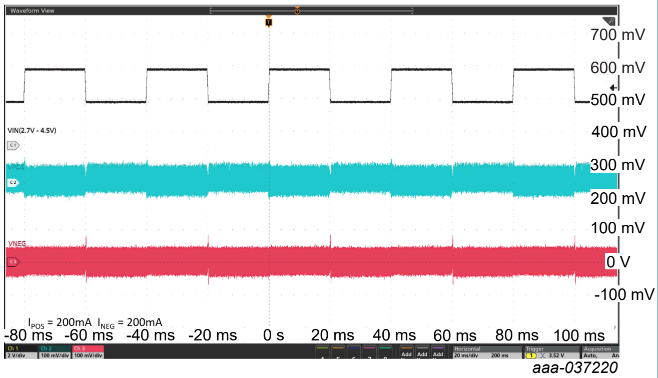
Fig. 37. Load transient



V_{IN} = 2.7 V to 4.5 V; $|V_{OUT}|$ = 5.4 V

I_{POS} = I_{NEG} = 0 mA

Fig. 38. Line transient



V_{IN} = 2.7 V to 4.5 V; $|V_{OUT}|$ = 5.4 V

I_{POS} = I_{NEG} = 200 mA

Fig. 39. Line transient

14. Detailed description

14.1. Overview

The NEX10001, supporting input voltage range from 2.7 V to 5 V, operates with a single inductor scheme to provide high efficiency with small solution size. The synchronous boost converter generates a positive voltage that is regulated down by an integrated Low Dropout (LDO) regulator, outputting the positive supply rail (V_{POS}). The negative supply rail (V_{NEG}) is generated by an integrated negative charge pump (CPN) driven from the boost converter output pin, REG.The device is programmable over an I²C compatible interface for both V_{POS} and V_{NEG}. The device topology allows a 100% asymmetry of the output voltages and currents.

14.2. Function block diagram

The NEX10001 function block diagram is shown in Fig. 40.

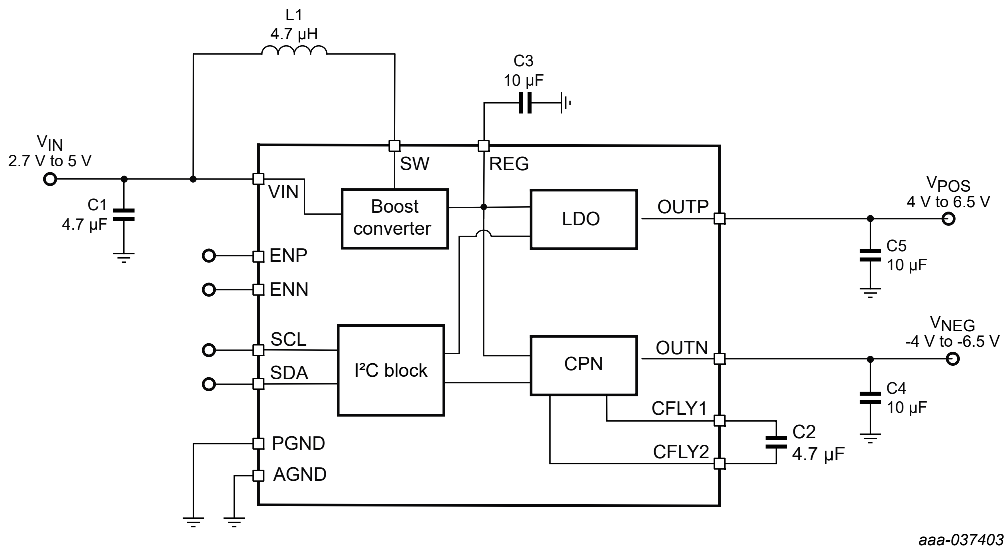


Fig. 40. Function block diagram

14.3. Feature description

14.3.1. Undervoltage lockout (UVLO)

The NEX10001 integrates an undervoltage lockout block (UVLO) that enables the device once the voltage on the VIN pin exceeds the UVLO threshold (2.5 V maximum). No output voltage will be generated if the enable signals are not pulled HIGH. The device, as well as all converters (boost converter, LDO, CPN), will be disabled as soon as the VIN voltage falls below the UVLO threshold. The UVLO threshold is designed with a hysteresis, the NEX10001 will continue operating as long as VIN stays above 2.25 V. This guarantees a proper operation even in the event of extensive line transients when the battery gets suddenly heavily loaded.

14.3.2. Thermal shutdown

The device has a build-in temperature sensor which monitors the internal junction temperature. When the junction temperature exceeds 140 °C, NEX10001 will shut down. When the junction temperature falls below the thermal recovery temperature, approximately 110 °C, the device restarts by using soft-start sequence.

14.3.3. Boost converter

14.3.3.1. Boost converter operation

The synchronous boost converter uses current mode topology with a typical switching frequency of 1.4 MHz, we recommend using 4.7 μH inductor. The converter is internally compensated and provides a regulated output voltage automatically adjusted depending on the programmed V_{POS} and V_{NEG} voltages. The boost converter operates either in continuous conduction mode (CCM) or Pulse Frequency Modulation mode (PFM), depending on the load current to provide the highest efficiency.

14.3.3.2. Power-up and soft-start (Boost Converter)

The Boost converter starts switching as soon as ENP or ENN is pulled high and the voltage on VIN pin is higher than UVLO threshold.

The boost converter starts up with internal soft start to avoid drawing excessive inrush current from the supply. The output voltage V_{REG} is slowly ramped up to its target value. Typical start-up waveforms for low-current applications are show in Fig. 32

14.3.3.3. Power-down (Boost Converter)

The boost converter stops switching when VIN is below the UVLO threshold or when both ENP and ENN are pulled low.

14.3.3.4. Output voltage (Boost Converter)

V_{REG}, the output voltage of boost converter is automatically adjusted according to the programmed V_{POS} and V_{NEG} voltages. V_{REG} will maintain a fixed voltage difference with the large values in V_{POS} and V_{NEG}.

14.3.3.5. Isolation (Boost Converter)

The boost converter output (REG) is isolated from the input supply VIN, providing a true shutdown.

14.3.4. LDO regulator

14.3.4.1. LDO operation

The Low Dropout regulator (LDO) generates the positive voltage rail, V_{POS}, by regulating down the output voltage of the boost converter (V_{REG}). The high PSRR LDO helps filtering the output ripple of the boost converter to provide low ripple V_{POS} voltage.

14.3.4.2. Power-up and soft-start (LDO)

The LDO starts operating as soon as the ENP signal is pulled HIGH and V_{IN} voltage is above the UVLO threshold and the boost converter has reached its Power Good threshold. In the case where the enable signal is already HIGH when V_{IN} exceeds the UVLO threshold, the boost converter will start first and the LDO will only start after the boost converter has reached its target voltage.

The LDO integrates a soft start that slowly ramps up its output voltage V_{POS} regardless of the output capacitor and the target voltage, as long as the LDO current limit is not reached, the typical start-up time is 540 µs. Typical start-up waveform for LDO are shown in Fig. 32.

14.3.4.3. Power-down and discharge (LDO)

The LDO stops operating when V_{IN} is below the UVLO threshold or when ENP is pulled LOW. The NEX10001 integrates actively discharge function for V_{POS}. Typical power down waveform for LDO is shown in Fig. 34.

14.3.4.4. Setting output voltage (LDO)

The output voltage of the LDO is programmable via I²C interface, from 4.0 V to 6.5 V in 100 mV steps. For more details, please refer to the V_{POS} register (address: 0x00)

14.3.4.5. Isolation (LDO)

The LDO isolates the V_{POS} rail from V_{REG} (boost converter output) as long as the rail is not enabled in order to ensure flexible start-up like V_{NEG} before V_{POS}.

14.3.5. Negative charge pump

14.3.5.1. CPN operation

The negative charge pump (CPN) generates the negative voltage rail, V_{NEG}, by inverting and regulating the output voltage of the boost converter (V_{REG}). The charge pump uses 4 switches and an external flying capacitor to generate the negative rail. Two of the switches are turned on in the first phase to charge the flying capacitor up to V_{REG}, and in the second phase they are turned-off and the two others turn on to pump the energy negatively out of the OUTN capacitor.

14.3.5.2. Power-up and soft-start (CPN)

The CPN starts operating as soon as the ENN signal is pulled HIGH and VIN voltage is above the UVLO threshold and the boost converter has reached its power good threshold. In the case where the enable signal is already HIGH when VIN reaches the UVLO threshold, the boost converter will start first and the CPN will only start after the boost converter has reached its target voltage. Typical startup waveform for CPN is shown in Fig. 32.

The CPN integrates a soft start that slowly ramps up its output voltage V_{NEG} within a time. The time is determined by the output voltage and the output capacitor value.

The estimated start-up time can be calculated using the following formula: $t_{\mathrm{STARTUP}} = \frac{C_{OUT} \times V_{NEG}}{I_{STARTUP}}$

Where:

- $t_{STARTUP}$ = start-up time of the V_{NEG} rail
- C_{OUT} = output capacitance of the V_{NEG} rail
- V_{NEG} = target output voltage
- $I_{STARTUP}$ = the output current of V_{NEG} to charge up the output capacitor at start-up

14.3.5.3. Power-down and discharge (CPN)

The CPN will stop operating when V_{IN} is below the UVLO threshold or when ENN is pulled LOW. NEX10001 integrates actively discharge function for V_{NEG}. Typical start-up waveform for V_{NEG} is shown in Fig. 32.

14.3.5.4. Setting output voltage (CPN)

The output voltage of the CPN is programmable via I²C interface, from -6.5 V to -4.0 V in 100 mV steps. For more details, please refer to the V_{NEG} register (address: 0x01).

14.3.5.5. Isolation (CPN)

The CPN isolates the V_{NEG} rail from V_{REG} (boost converter output) as long as the rail is not enabled in order to ensure flexible start-up like V_{POS} before V_{NEG}.

14.3.6. I²C serial interface

NEX10001 integrates an industry standard I²C compatible interface as a slave. The slave address is 0x3E.

14.3.7. Register configuration

Table 10. Register map

Address	Register name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00[1]	V_{POS} register	R/W	reserved			V_{POS} [4:0]					0x0E
0x01[1]	V_{NEG} register	R/W	reserved			V_{NEG} [4:0]					0x0E
0x2	CL and Vendor ID	R/W	reserved			LDO_CL	reserved		11		0x03

[1] 0x00 and 0x01: the relationship between V_{POS}, V_{NEG} registers and V_{POS}, V_{NEG} voltages are shown in Table 11.

Table 11. V_{POS} and V_{NEG} voltages

V_{POS} [4:0]	V_{POS} voltage	V_{NEG} [4:0]	V_{NEG} voltage
0x00	4.0	0x00	-4.0
0x01	4.1	0x01	-4.1
0x02	4.2	0x02	-4.2
0x03	4.3	0x03	-4.3
0x04	4.4	0x04	-4.4
0x05	4.5	0x05	-4.5
0x06	4.6	0x06	-4.6
0x07	4.7	0x07	-4.7
0x08	4.8	0x08	-4.8
0x09	4.9	0x09	-4.9
0x0A	5.0	0x0A	-5.0
0x0B	5.1	0x0B	-5.1
0x0C	5.2	0x0C	-5.2
0x0D	5.3	0x0D	-5.3
0x0E	5.4 (Default value)	0x0E	-5.4 (Default value)
0x0F	5.5	0x0F	-5.5
0x10	5.6	0x10	-5.6
0x11	5.7	0x11	-5.7
0x12	5.8	0x12	-5.8
0x13	5.9	0x13	-5.9
0x14	6.0	0x14	-6.0
0x15	6.1	0x15	-6.1
0x16	6.2	0x16	-6.2

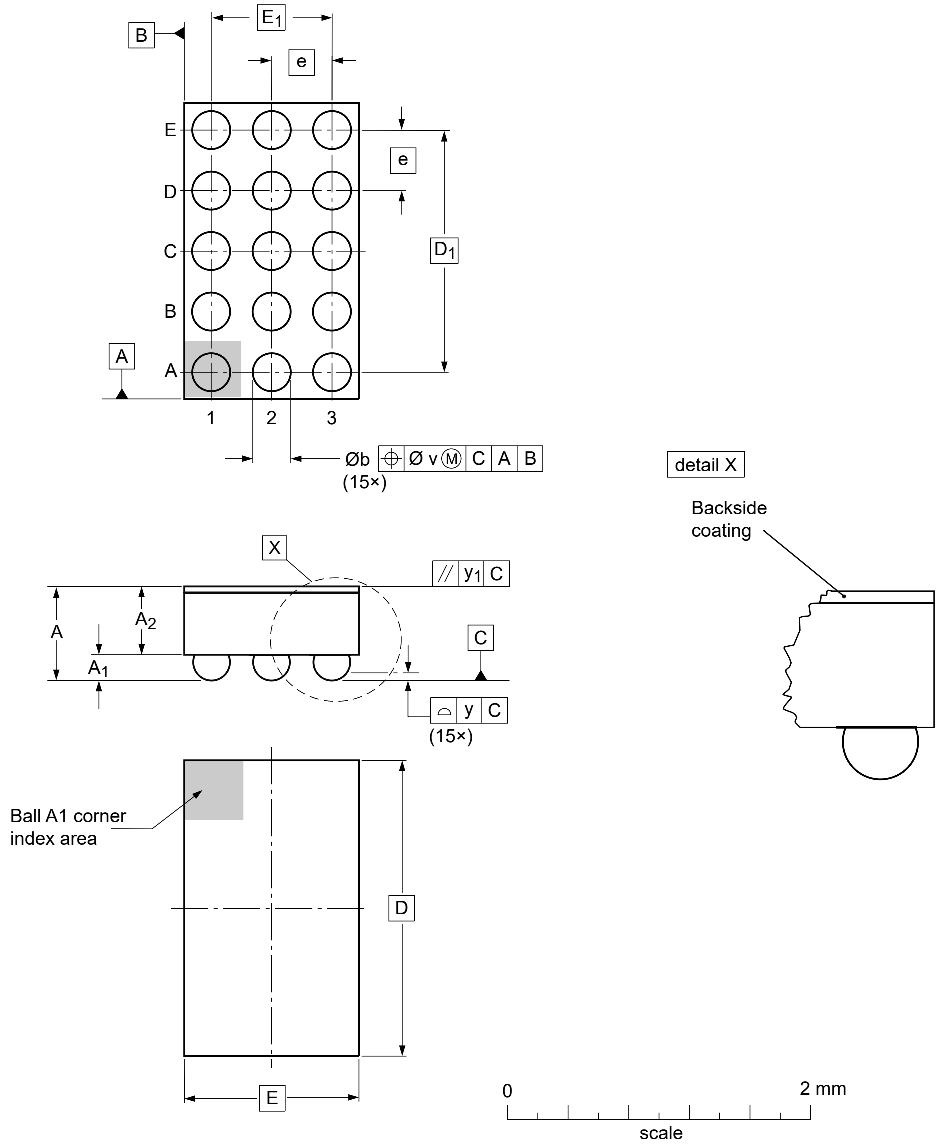
V_{POS} [4:0]	V_{POS} voltage	V_{NEG} [4:0]	V_{NEG} voltage
0x17	6.3	0x17	-6.3
0x18	6.4	0x18	-6.4
0x19	6.5	0x19	-6.5

Table 12. Definition of 0x02 register

Bit	Field	Description	Value	Action
7:5	Reserved	Reserved	Reserved	Reserved
4	LDO_CL	V_{POS} current limit	0	current limit 280 mA
			1	current limit 370 mA
3:2	Reserved	Reserved	Reserved	Reserved
1:0	Vender ID	Vendor ID	11	Read only Vender ID

15. Package outline

WLCSP15: wafer level chip-scale package; 15 bumps; 1.16 × 1.96 × 0.62 mm body **SOT8054-1**



Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	A_2	b	D	D_1	E	E_1	e	u	v	y	y_1
mm	max	0.66	0.19	0.47	0.264	1.96 BSC	1.6 BSC	1.16 BSC	0.8 BSC	0.4 BSC	0.03	0.015	0.05	0.06
	nom	0.62	0.17	0.45	0.244									
	min	0.58	0.15	0.43	0.224									

sot8054-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8054-1						~~23-04-11~~ 23-06-15

Fig. 41. Package outline SOT8054-1 (WLCSP15)

16. Abbreviations

Table 13. Abbreviations

Acronym	Description
CCM	Continuous Conduction Mode
CDM	Charged Device Model
CPN	Negative Charge Pump
ESD	ElectroStatic Discharge
HBM	Human Body Model
LDO	Low Dropout
OTSD	Over Temperature Shut Down
PCB	Printed Circuit Board
PFM	Pulse Frequency Modulation
PSRR	Power Supply Rejection Ratio
TFT-LCD	Thin Film Transistor-Liquid Crystal Display
UVLO	Undervoltage Lockout

17. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NEX10001UB v. 2	20231220	Product data sheet	-	NEX10001UB v. 1
Modifications:	• Section 5: marking code has changed			
NEX10001UB v. 1	20231106	Product data sheet	-	-

18. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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