



PDTA114EM

50 V, 100 mA PNP resistor-equipped transistor;
R1 = 10 k Ω , R2 = 10 k Ω

19 February 2024

Product data sheet

1. General description

PNP Resistor-Equipped Transistor (RET) in a leadless ultra small SOT883 (SC-101) Surface-Mounted Device (SMD) plastic package.

NPN complement: PDTC114EM

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

3. Applications

- Digital application in automotive and industrial segments
- Cost-saving alternative for BC847 series in digital applications
- Controlling IC inputs
- Switching loads

4. Quick reference data

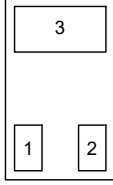
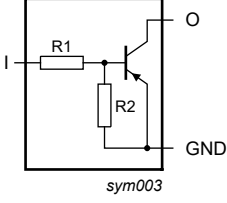
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{CEO}	collector-emitter voltage	open base		-	-	-50	V
I _O	output current			-	-	-100	mA
R1	bias resistor 1 (input)		[1]	7	10	13	k Ω
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	

[1] See "Section 11: Test information" for resistor calculation and test conditions.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 <p>Transparent top view</p> <p>DFN1006-3 (SOT883)</p>	 <p>sym003</p>
2	GND	ground (emitter)		
3	O	output (collector)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PDTA114EM	DFN1006-3	plastic, leadless ultra small package; 3 terminals; 0.35 mm pitch; 1 mm x 0.6 mm x 0.48 mm body	SOT883

7. Marking

Table 4. Marking codes

Type number	Marking code
PDTA114EM	E5

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter	-	-50	V
V_{CEO}	collector-emitter voltage	open base	-	-50	V
V_{EBO}	emitter-base voltage	open collector	-	-10	V
V_I	input voltage		-40	10	V
I_O	output current		-	-100	mA
I_{CM}	peak collector current	$t_p \leq 1$ ms; single pulse	-	-100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1] [2]	250	mW
T_j	junction temperature		-	150	°C
T_{amb}	ambient temperature		-65	150	°C
T_{stg}	storage temperature		-65	150	°C

[1] Reflow soldering is the only recommended soldering method.

[2] Device mounted on an FR4 PCB with 70 μm copper strip line, standard footprint.

50 V, 100 mA PNP resistor-equipped transistor; R1 = 10 kΩ, R2 = 10 kΩ

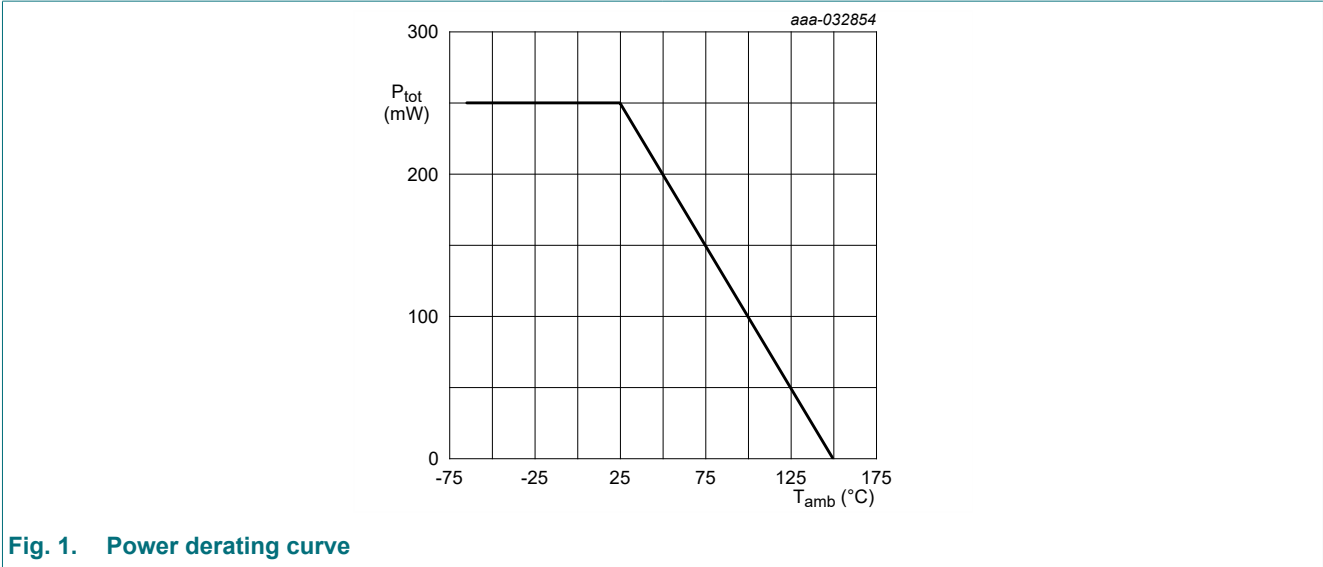


Fig. 1. Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	500	K/W

- [1] Reflow soldering is the only recommended soldering method.
- [2] Device mounted on an FR4 PCB with 70 μm copper strip line, standard footprint.

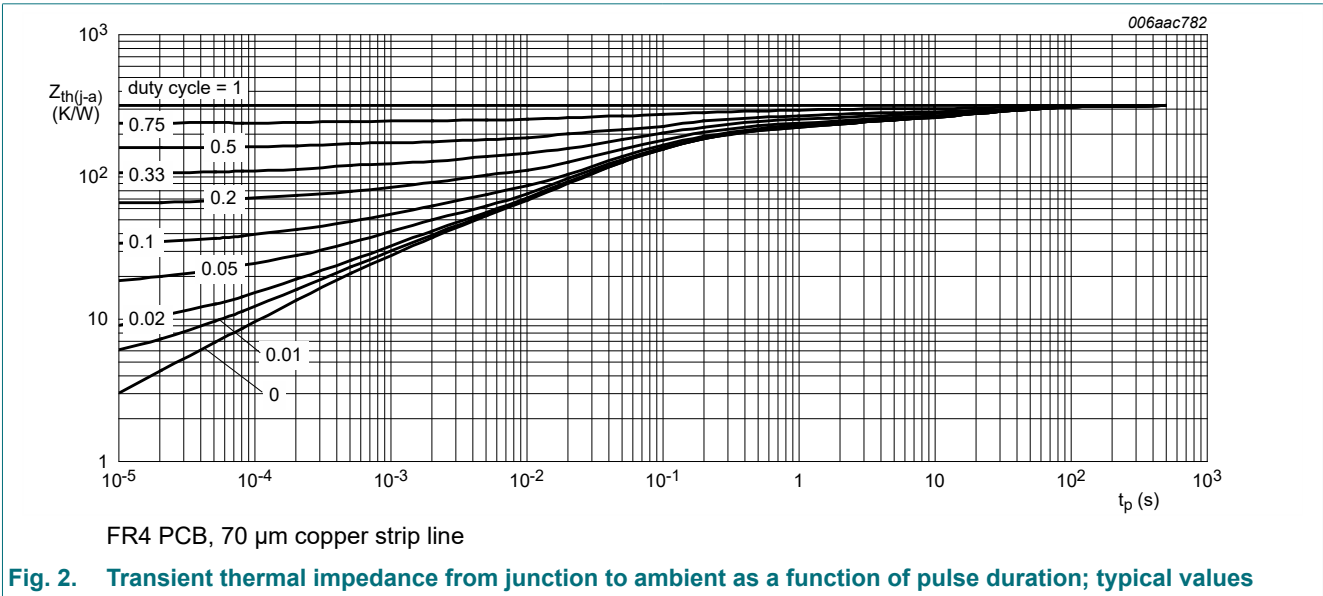


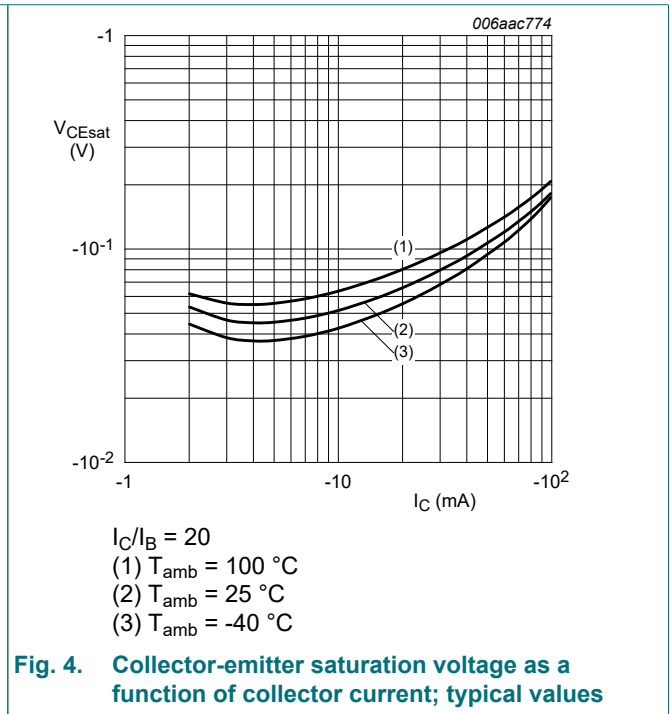
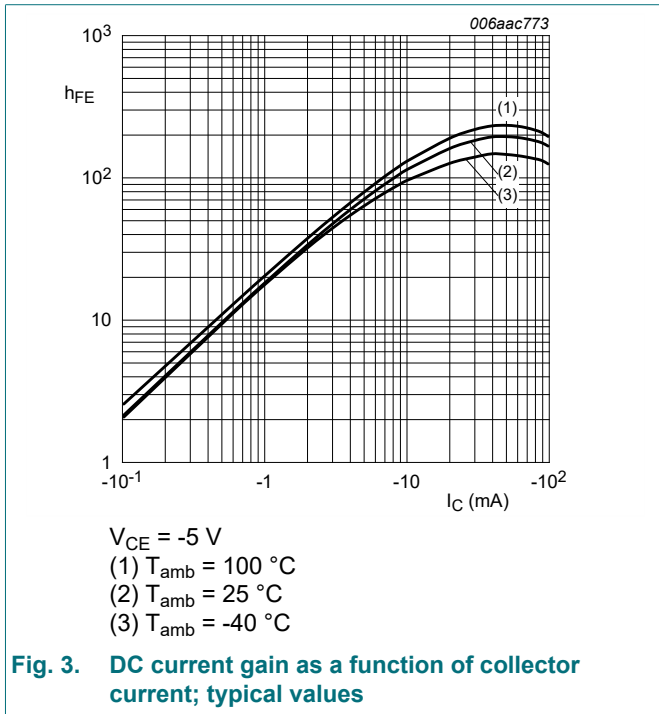
Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

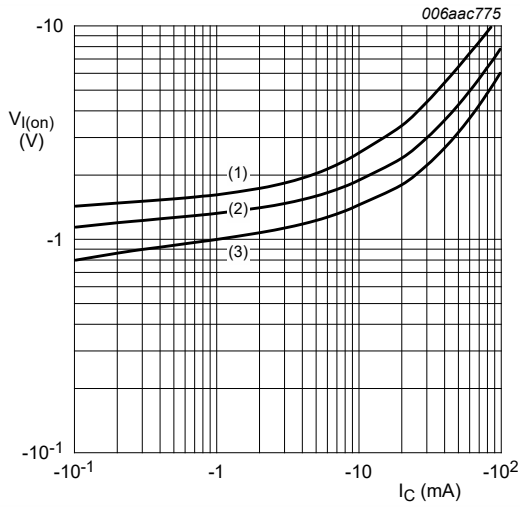
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = -100 \mu A$; $I_E = 0 A$; $T_{amb} = 25 \text{ }^\circ C$	-50	-	-	V	
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = -2 \text{ mA}$; $I_B = 0 A$; $T_{amb} = 25 \text{ }^\circ C$	-50	-	-	V	
I_{CBO}	collector-base cut-off current	$V_{CB} = -50 \text{ V}$; $I_E = 0 A$; $T_{amb} = 25 \text{ }^\circ C$	-	-	-100	nA	
I_{CEO}	collector-emitter cut-off current	$V_{CE} = -30 \text{ V}$; $I_B = 0 A$; $T_{amb} = 25 \text{ }^\circ C$	-	-	-1	μA	
		$V_{CE} = -30 \text{ V}$; $I_B = 0 A$; $T_j = 150 \text{ }^\circ C$	-	-	-5	μA	
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5 \text{ V}$; $I_C = 0 A$; $T_{amb} = 25 \text{ }^\circ C$	-	-	-400	μA	
h_{FE}	DC current gain	$V_{CE} = -5 \text{ V}$; $I_C = -5 \text{ mA}$; $T_{amb} = 25 \text{ }^\circ C$	30	-	-		
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10 \text{ mA}$; $I_B = -0.5 \text{ mA}$; $T_{amb} = 25 \text{ }^\circ C$	-	-	-150	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5 \text{ V}$; $I_C = -100 \mu A$; $T_{amb} = 25 \text{ }^\circ C$	-	-1.1	-0.8	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = -0.3 \text{ V}$; $I_C = -10 \text{ mA}$; $T_{amb} = 25 \text{ }^\circ C$	-2.5	-1.8	-	V	
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
C_c	collector capacitance	$V_{CB} = -10 \text{ V}$; $I_E = 0 A$; $i_e = 0 A$; $f = 1 \text{ MHz}$; $T_{amb} = 25 \text{ }^\circ C$	-	-	3	pF	
f_T	transition frequency	$V_{CE} = -5 \text{ V}$; $I_C = -10 \text{ mA}$; $f = 100 \text{ MHz}$; $T_{amb} = 25 \text{ }^\circ C$	[2]	-	180	-	MHz

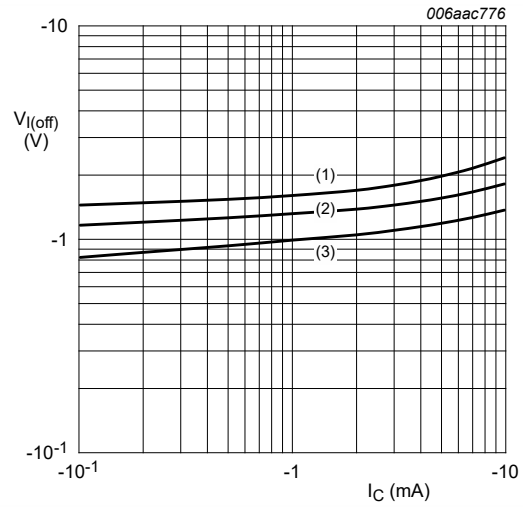
- [1] See "Section 11: Test information" for resistor calculation and test conditions.
 [2] Characteristics of built-in transistor.





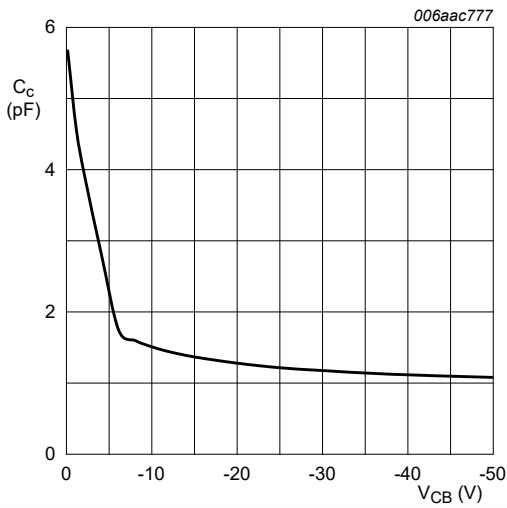
$V_{CE} = -0.3 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig. 5. On-state input voltage as a function of collector current; typical values



$V_{CE} = -5 \text{ V}$
 (1) $T_{amb} = -40 \text{ }^\circ\text{C}$
 (2) $T_{amb} = 25 \text{ }^\circ\text{C}$
 (3) $T_{amb} = 100 \text{ }^\circ\text{C}$

Fig. 6. Off-state input voltage as a function of collector current; typical values



$f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 7. Collector capacitance as a function of collector-base voltage; typical values

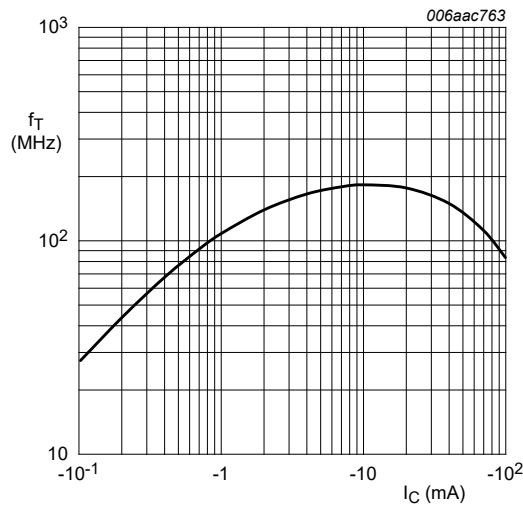


Fig. 8. Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_3)}{R_1 \cdot I_3} - 1$$

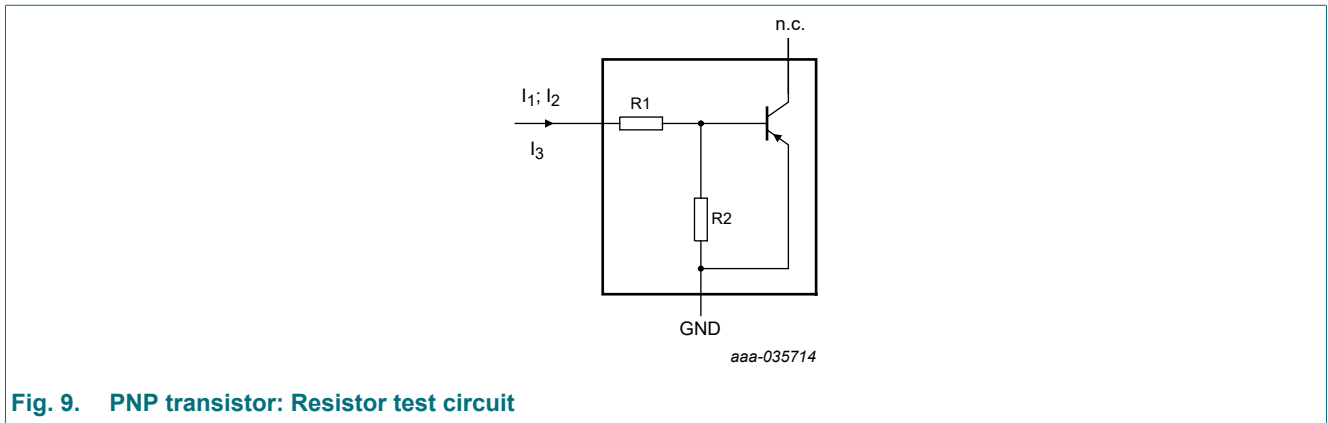


Fig. 9. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions		
			I1	I2	I3
PDTA114EM	10	10	-350 μA	-450 μA	400 μA

12. Package outline

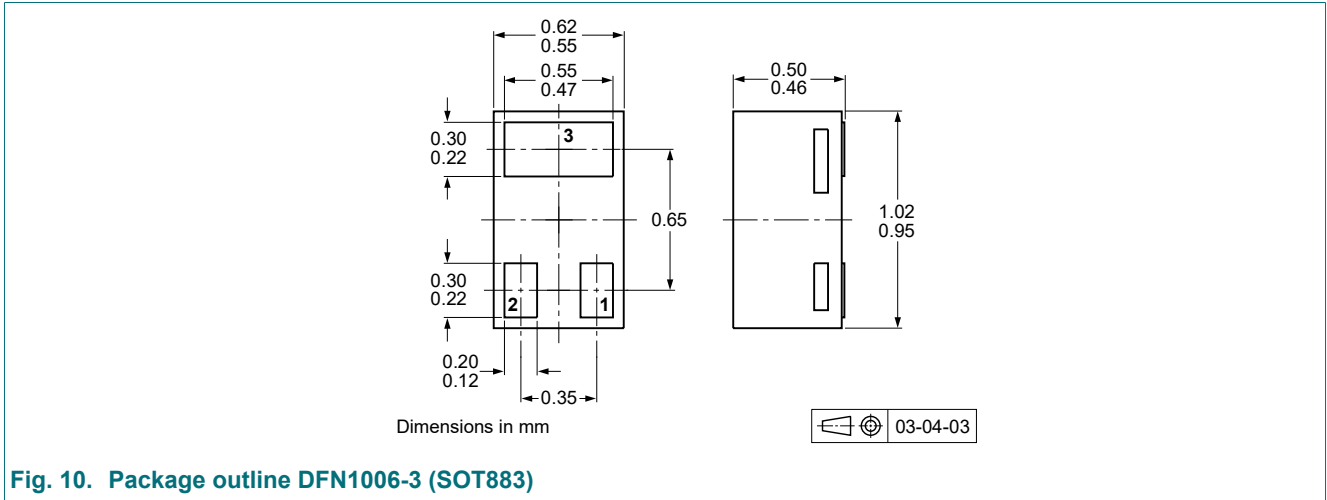


Fig. 10. Package outline DFN1006-3 (SOT883)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTA114EM v.12	20240219	Product data sheet	-	PDTA114E_SER v.11
Modification:	<ul style="list-style-type: none"> Pinning: Graphic symbol adjusted 			
PDTA114EM v.11	20230207	Product data sheet	-	PDTA114E_SER v.10
PDTA114E_SER v.10	20111221	Product data sheet	-	PDTA114E_SER v.9
PDTA114E_SER v.9	20111122	Product data sheet	-	PDTA114E_SERIES v.8
PDTA114E_SERIES v.8	20040802	Product specification	-	PDTA114E_SERIES v.7
PDTA114E_SERIES v.7	20030410	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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