

# PDTA115EU-Q

PNP resistor-equipped transistor; R1 = 100 kΩ, R2 = 100 kΩ

1 March 2024

Product data sheet

## 1. General description

PNP Resistor-Equipped Transistor (RET) in a very small SOT323 (SC-70) Surface-Mounted Device (SMD) plastic package.

#### 2. Features and benefits

- · Built-in bias resistors
- · Simplifies circuit design
- · Reduces component count
- Reduces pick and place costs
- Qualified according to AEC-Q101 and recommended for use in automotive applications

## 3. Applications

- · General purpose switching and amplification
- · Inverter and interface circuits
- · Circuit driver

### 4. Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	-50	V
Io	output current		-	-	-20	mA
R1	bias resistor 1 (input)	T <sub>amb</sub> = 25 °C	70	100	130	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	

## 5. Pinning information

**Table 2. Pinning information** 

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	<u></u> 3	
2	G	GND (emitter)		0
3	0	output (collector)	1 2 SC-70 (SOT323)	R2 GND sym003



PNP resistor-equipped transistor; R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$ 

## 6. Ordering information

#### **Table 3. Ordering information**

Type number	Package						
	Name	Description	Version				
PDTA115EU-Q	SC-70	plastic, surface-mounted package; 3 leads; 1.3 mm pitch; 2 mm x 1.25 mm x 0.95 mm body	SOT323				

## 7. Marking

#### Table 4. Marking codes

Type number	Marking code[1]
PDTA115EU-Q	%7C

<sup>[1] % =</sup> placeholder for manufacturing site code

## 8. Limiting values

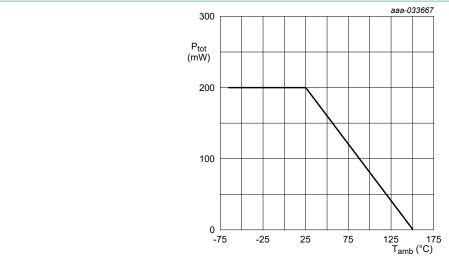
#### **Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CBO}$	collector-base voltage	open emitter		-	-50	V
$V_{CEO}$	collector-emitter voltage	open base		-	-50	V
$V_{EBO}$	emitter-base voltage	open collector		-	-10	V
VI	input voltage			-40	10	V
Io	output current			-	-20	mA
I <sub>CM</sub>	peak collector current			-	-100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	200	mW
Tj	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-65	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

<sup>[1]</sup> Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

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FR4 PCB, single-sided, 35  $\mu m$  copper, tin-plated and standard footprint

Fig. 1. Power derating curve

#### 9. Thermal characteristics

**Table 6. Thermal characteristics** 

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
""(J-a)	thermal resistance from junction to ambient	T <sub>amb</sub> ≤ 25 °C	[1]	-	-	625	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

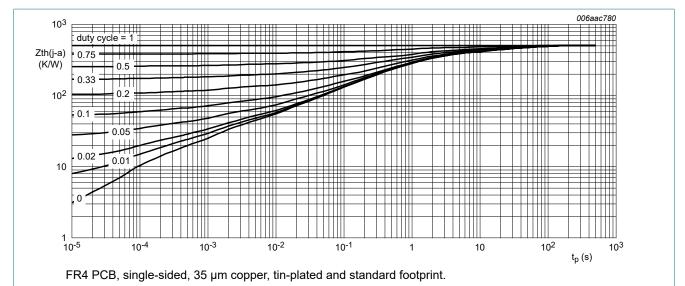


Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

PNP resistor-equipped transistor; R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$ 

## 10. Characteristics

**Table 7. Characteristics** 

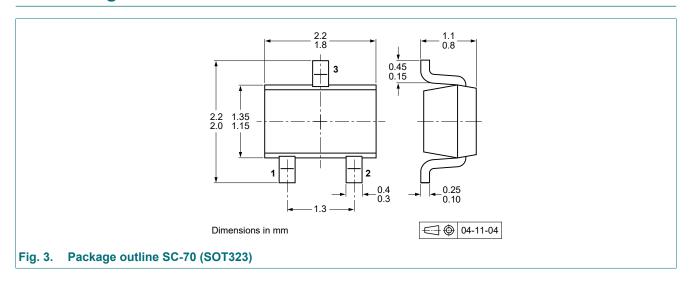
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = -50 V; I <sub>E</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	-100	nA
I <sub>CEO</sub>	collector-emitter cut-off	V <sub>CE</sub> = -30 V; I <sub>B</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	-100	nA
	current	V <sub>CE</sub> = -30 V; I <sub>B</sub> = 0 A; T <sub>j</sub> = 150 °C	-	-	-5	μΑ
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = -5 V; I <sub>C</sub> = 0 A; T <sub>amb</sub> = 25 °C	-	-	-50	μΑ
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = -5 V; I <sub>C</sub> = -5 mA; T <sub>amb</sub> = 25 °C	80	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	$I_C = -5 \text{ mA}$ ; $I_B = -0.25 \text{ mA}$ ; $T_{amb} = 25 ^{\circ}\text{C}$	-	-	-150	mV
V <sub>I(off)</sub>	off-state input voltage	V <sub>CE</sub> = -5 V; I <sub>C</sub> = -100 μA; T <sub>amb</sub> = 25 °C	-	-1.2	-0.5	V
V <sub>I(on)</sub>	on-state input voltage	$V_{CE} = -0.3 \text{ V}; I_{C} = -1 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$	-3	-1.6	-	V
R1	bias resistor 1 (input)	T <sub>amb</sub> = 25 °C	70	100	130	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	
C <sub>c</sub>	collector capacitance	$V_{CB}$ = -10 V; $I_{E}$ = 0 A; $i_{e}$ = 0 A; $f$ = 1 MHz; $T_{amb}$ = 25 °C	-	-	3	pF

### 11. Test information

### **Quality information**

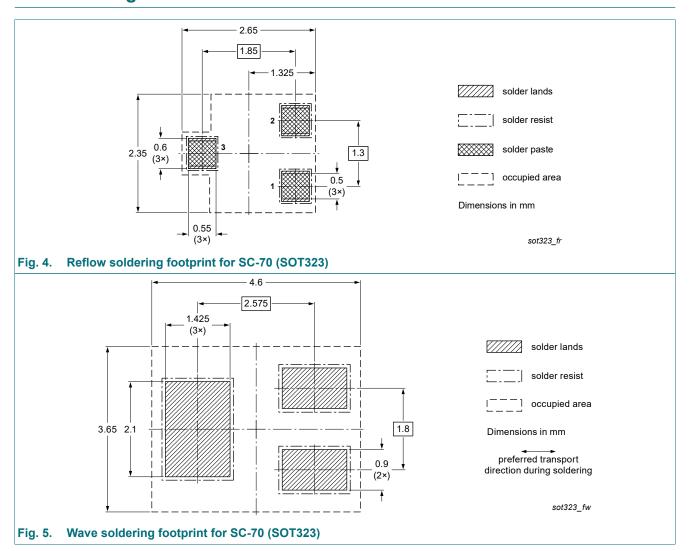
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 12. Package outline



PNP resistor-equipped transistor; R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$ 

## 13. Soldering



PNP resistor-equipped transistor; R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$ 

## 14. Revision history

#### Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTA115EU-Q v.1	20240301	Product data sheet	-	-

#### PNP resistor-equipped transistor; R1 = 100 k $\Omega$ , R2 = 100 k $\Omega$

### 15. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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