

PDTC114YU

50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 47 k Ω

25 April 2023

Product data sheet

1. General description

NPN Resistor-Equipped Transistor (RET) in a very small SOT323 (SC-70) Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTA114YU

2. Features and benefits

- 100 mA output current capability
- · Built-in bias resistors
- · Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

3. Applications

- · Digital application in industrial segments
- Cost-saving alternative for BC847 series in digital applications
- · Controlling IC inputs
- Switching loads

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{CEO}	collector-emitter voltage	open base		-	-	50	V
Io	output current			-	-	100	mA
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	3.7	4.7	5.7	

[1] See "Section 11: Test information" for resistor calculation and test conditions.



50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 47 k Ω

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	3	
2	GND	ground (emitter)		R1 P
3	0	output (collector)	1 2 SC-70 (SOT323)	GND Sym007

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PDTC114YU	SC-70	plastic, surface-mounted package; 3 leads; 1.3 mm pitch; 2 mm x 1.25 mm x 0.95 mm body	SOT323			

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PDTC114YU	%30

^{[1] % =} placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

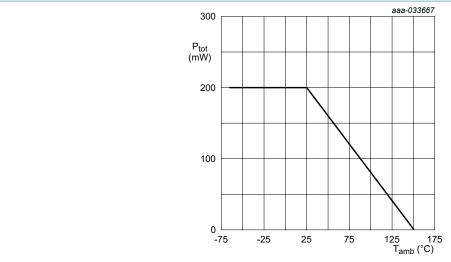
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	6	V
VI	input voltage			-6	40	V
Io	output current			-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	200	mW
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

 $^{[1] \}quad \text{Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 } \mu\text{m copper, tin-plated and standard footprint.}$

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FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint

Fig. 1. Power derating curve

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.

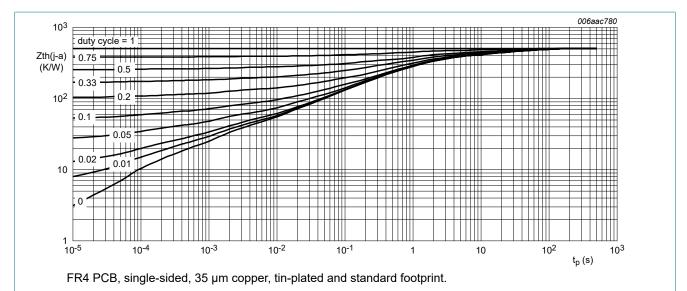


Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

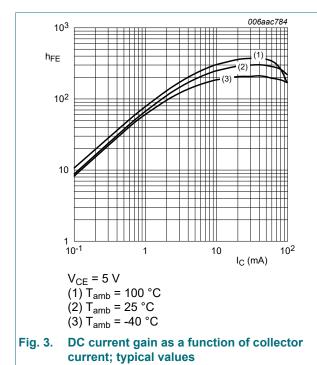
50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 47 k Ω

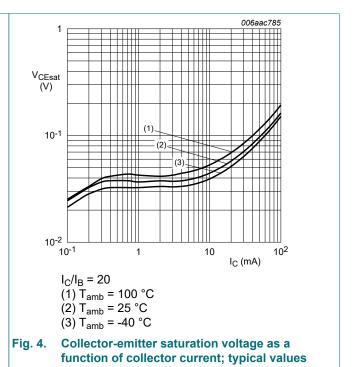
10. Characteristics

Table 7. Characteristics

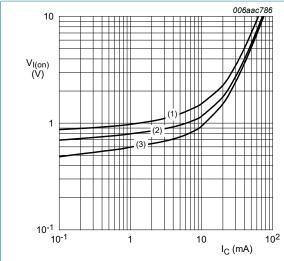
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{(BR)CBO}	collector-base breakdown voltage	$I_C = 100 \ \mu A; I_E = 0 \ A; T_{amb} = 25 \ ^{\circ}C$		50	-	-	V
V _{(BR)CEO}	collector-emitter breakdown voltage	= 2 mA; I _B = 0 A; T _{amb} = 25 °C		50	-	-	V
I _{CBO}	collector-base cut-off current	_{CB} = 50 V; I _E = 0 A; T _{amb} = 25 °C		-	-	100	nA
I _{CEO}	collector-emitter cut-off	V _{CE} = 30 V; I _B = 0 A; T _{amb} = 25 °C		-	-	100	nA
	current	V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C		-	-	5	μΑ
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A; T _{amb} = 25 °C		-	-	150	μΑ
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 5 mA; T _{amb} = 25 °C		100	-	-	
V _{CEsat}	collector-emitter saturation voltage	$I_C = 5 \text{ mA}; I_B = 0.25 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$		-	-	100	mV
V _{I(off)}	off-state input voltage	V _{CE} = 5 V; I _C = 100 μA; T _{amb} = 25 °C		-	0.7	0.5	V
V _{I(on)}	on-state input voltage	V _{CE} = 0.3 V; I _C = 1 mA; T _{amb} = 25 °C		1.4	0.8	-	V
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	3.7	4.7	5.7	
C _c	collector capacitance	V_{CB} = 10 V; I_{E} = 0 A; i_{e} = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	2.5	pF
f _T	transition frequency	V_{CE} = 5 V; I_{C} = 10 mA; f = 100 MHz; T_{amb} = 25 °C	[2]	-	230	-	MHz

- [1] See "Section 11: Test information" for resistor calculation and test conditions.
- [2] Characteristics of built-in transistor.





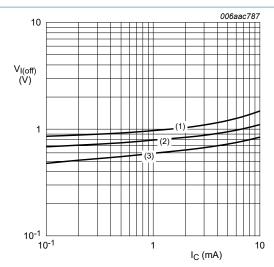
50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 47 k Ω



 $V_{CE} = 0.3 V$

(1) T_{amb} = -40 °C (2) T_{amb} = 25 °C (3) T_{amb} = 100 °C

Fig. 5. On-state input voltage as a function of collector | Fig. 6. current; typical values



V_{CE} = 5 V (1) T_{amb} = -40 °C (2) T_{amb} = 25 °C (3) T_{amb} = 100 °C

Off-state input voltage as a function of collector current; typical values

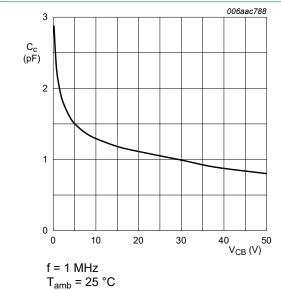
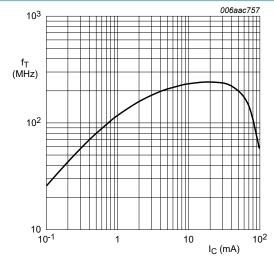


Fig. 7. Collector capacitance as a function of collectorbase voltage; typical values



 V_{CE} = 5 V; T_{amb} = 25 °C

Fig. 8. Transition frequency as a function of collector current; typical values of built-in transistor

50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 47 k Ω

11. Test information

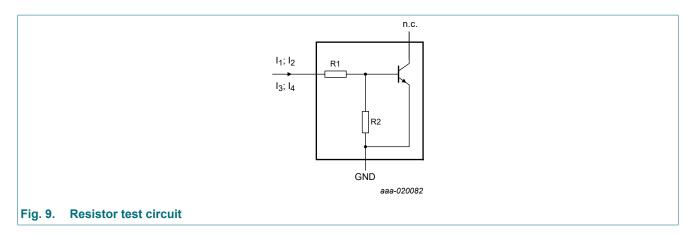
Resistor calculation

· Calculation of bias resistor 1 (R1)

$$R_{I} = \frac{V(I_{2}) - V(I_{1})}{I_{2} - I_{1}}$$

· Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I4) - V(I3)}{R1 \cdot (I4 - I3)} - 1$$

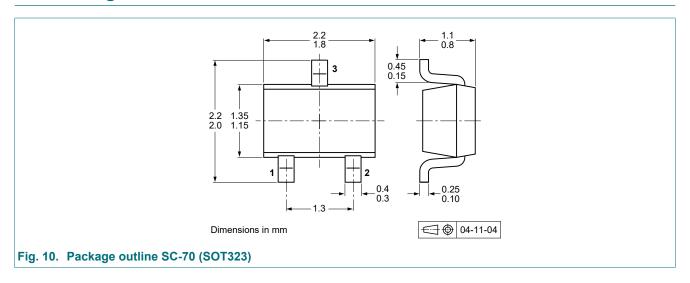


Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I ₁	l ₂	l ₃	14
PDTC114YU	10	47	90 μΑ	140 µA	-55 μΑ	-105 µA

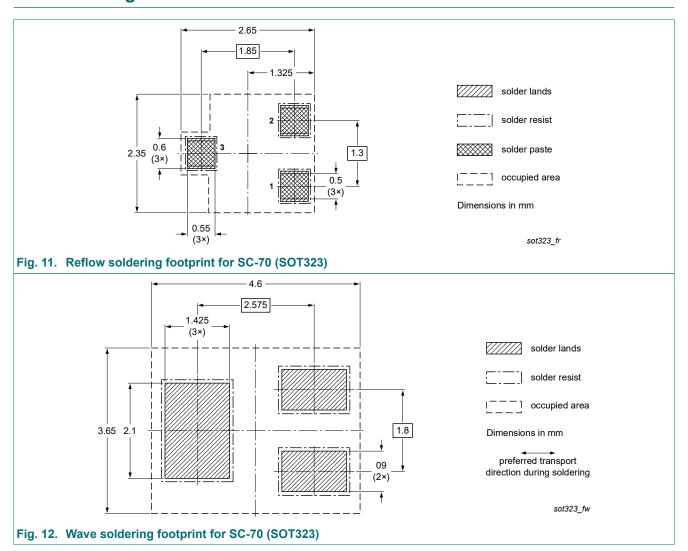
12. Package outline



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50 V, 100 mA NPN resistor-equipped transistor; R1 = 10 k Ω , R2 = 47 k Ω

13. Soldering



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14. Revision history

Table 9. Revision history

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Data sheet ID	Release date	Data sheet status	Change notice	Supersedes	
PDTC114YU v.8	20230425	Product data sheet	-	PDTC114Y_SER v.7	
Modification:	 Family data sheet reduced to single type data sheet. The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Product changed to non automotive. Please refer to the automotive product(s) with -Q. Packing information removed. Characteristics: Value corrected for I_{CEO} at 25°C. 				
PDTC114Y_SER v.7	20111118	Product data sheet	-	PDTC114Y_SERIES v.6	
PDTC114Y_SERIES v.6	20040817	Product data sheet	-	PDTC114Y_SERIES v.5	
PDTC114Y_SERIES v.5	20040910	Product specification	-	PDTC114Y_SERIES v.4	
PDTC114Y_SERIES v.4	20030414	Product specification	-	-	

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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