Product data sheet

1. General description

Ultra low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode in a DFN1006-2 (SOD882) leadless ultra small Surface-Mounted Device (SMD) plastic package, designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of one line
- High reverse standoff voltage V_{RWM} = 30 V
- Ultra-low diode capacitance C_d = 0.27 pF
- Ultra small plastic package 1.0 x 0.6 x 0.48 mm
- ESD protection up to ±12 kV contact discharge according to IEC 61000-4-2

3. Applications

- NFC antenna protection
- · Protection of high-speed data lines

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C	-	-	30	V
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C	-	0.27	0.35	pF



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)		
2	K2	cathode (diode 2)	Transparent top view DFN1006-2 (SOD882)	K1 K2

6. Ordering information

Table 3. Ordering information

ype number Package					
	Name	Description	Version		
PESD30VF1BBL	DFN1006-2	plastic, leadless ultra small package; 2 terminals; 0.65 mm pitch; 1 mm x 0.6 mm x 0.48 mm body	SOD882		

7. Marking

Table 4. Marking codes

Type number	Marking code		
PESD30VF1BBL	% %		

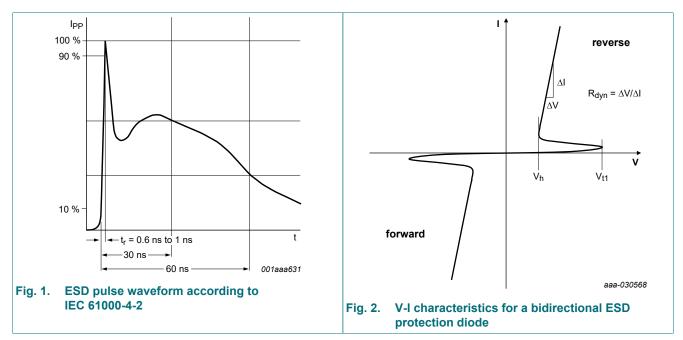
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximu	ım ratings		·	·		
V _{ESD}	electrostatic discharge	IEC 61000-4-2; contact discharge	[1]	-	12	kV
	voltage	IEC 61000-4-2; air discharge	[1]	-	15	kV

[1] Device stressed with ten non-repetitive ESD pulses.



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	30	V
V_{BR}	breakdown voltage	I _R = 10 mA; T _{amb} = 25 °C		31	35	-	V
I _{RM}	reverse leakage current	V _R = 30 V; T _{amb} = 25 °C		-	1	30	nA
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C		-	0.27	0.35	pF
V _{CL}	clamping voltage	I _{TLP} = 8 A; t _p = 100 ns; T _{amb} = 25 °C	[1]	-	18.5	-	V
		I _{TLP} = 16 A; t _p = 100 ns; T _{amb} = 25 °C	[1]	-	21	-	V
R _{dyn}	dynamic resistance	$I_R = 7.5 \text{ A}; t_p = 100 \text{ ns}; T_{amb} = 25 ^{\circ}\text{C}$	[1]	-	8.0	-	Ω

[1] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.

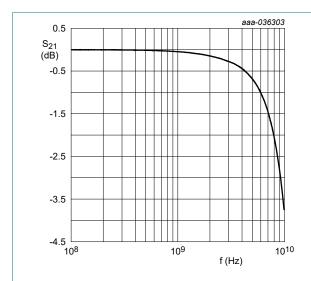


Fig. 3. Insertion loss; typical values

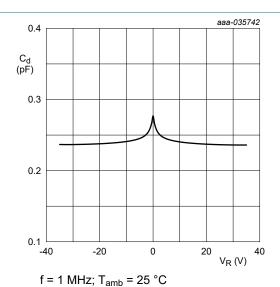
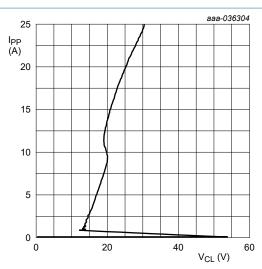
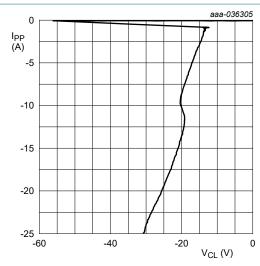


Fig. 4. Capacitance as a function of reverse voltage; typical values



Transmission Line Pulse (TLP); $t_p = 100 \text{ ns}$; $t_r = 1 \text{ ns}$

Fig. 5. Dynamic resistance with positive clamping; typical values



Transmission Line Pulse (TLP); $t_p = 100 \text{ ns}$; $t_r = 1 \text{ ns}$

Fig. 6. Dynamic resistance with negative clamping; typical values

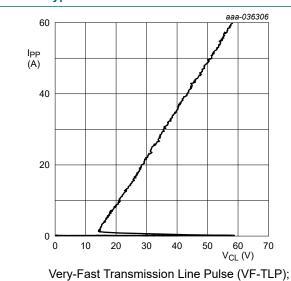
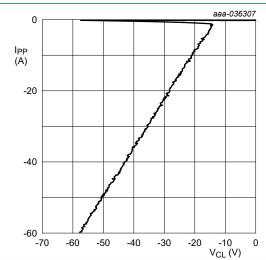


Fig. 7. Dynamic resistance with positive clamping; typical values

 $t_p = 5 \text{ ns}; t_r = 600 \text{ ps}$



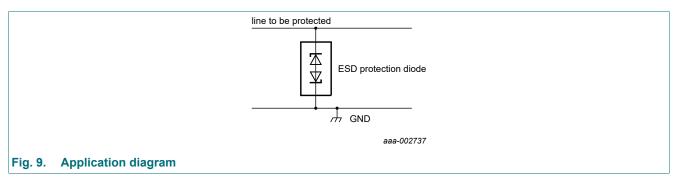
Very-Fast Transmission Line Pulse (VF-TLP); $t_p = 5 \text{ ns}$; $t_r = 600 \text{ ps}$

Fig. 8. Dynamic resistance with negative clamping; typical values

10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

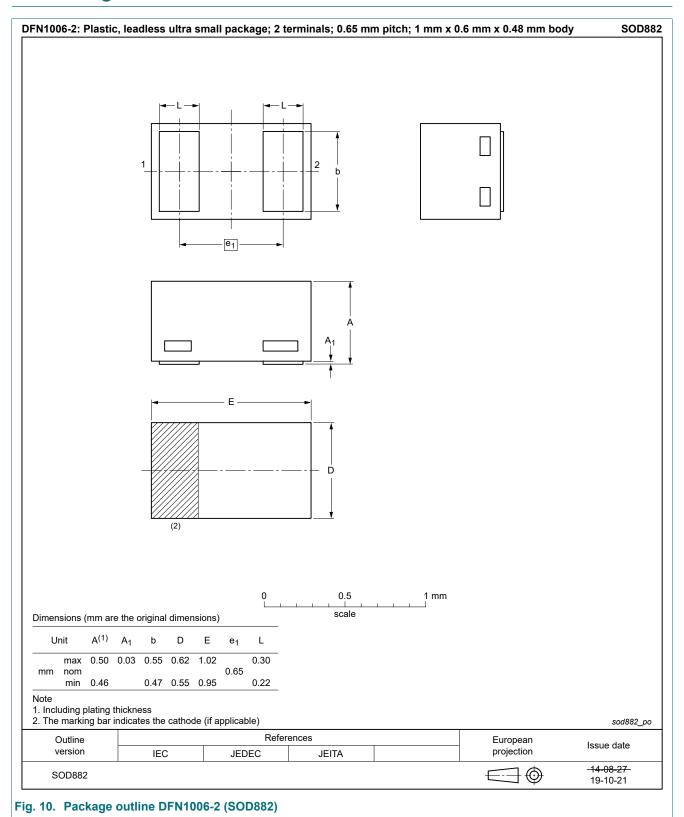


Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

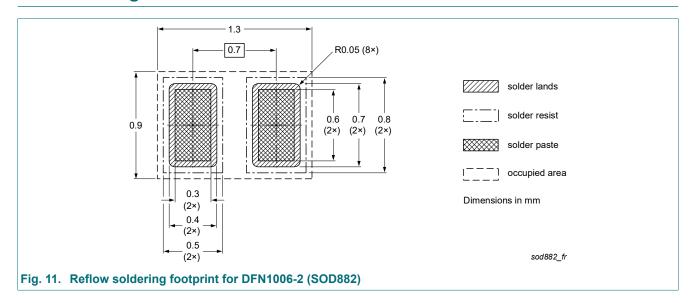
- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- **6.** Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline



7/11

12. Soldering



13. Revision history

Table 7. Revision history

Table 1. Revision misto	ı y			
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD30VF1BBL v.2	20230725	Product data sheet	-	PESD30VF1BBL v.1
Modifications:	Chapter "Limiting valChapter "Limiting val	nent to non-automotive qu lues": IEC 61000-4-2 con lues": IEC 61000-4-2 air ond benefits": ESD informa	tact discharge revised discharge revised	
PESD30VF1BBL v.1	20230608	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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