



# PSMN2R5-80SSE

N-channel 80 V, 2.5 mOhm MOSFET with enhanced SOA in LPAK88

15 March 2024

Preliminary data sheet

## 1. General description

N-channel enhancement mode MOSFET in a LPAK88 package qualified to 175 °C. Part of Nexperia's Application Specific MOSFETs (ASFETs) for Hotswap and Soft Start. The PSMN2R5-80SSE delivers very low  $R_{DS(on)}$  and enhanced safe operating area performance in a high-reliability copper-clip LPAK88 package.

PSMN2R5-80SSE complements the latest "hot-swap" controllers – robust enough to withstand substantial inrush currents during turn-on, low  $R_{DS(on)}$  to minimize  $I^2R$  losses and deliver optimum efficiency when turned fully ON.

## 2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low  $R_{DS(on)}$  for low  $I^2R$  conduction losses
- LPAK88 package for applications that demand the highest performance and reliability

## 3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	-	225	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	341	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 12</a>	-	2	2.5	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 40\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	4	13.4	31	nC
$Q_{G(tot)}$	total gate charge		58	116	174	nC
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 82\text{ A}$ ; $V_{sup} \leq 80\text{ V}$ ; $R_{GS} = 50\text{ Ω}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; $t_p = 147\text{ μs}$ ; <a href="#">Fig. 4</a>	[1]	-	628	mJ

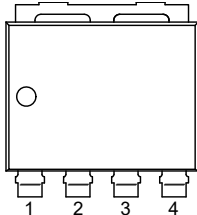
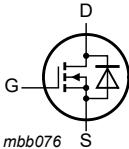
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
Q <sub>r</sub>	recovered charge	I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 40 V; <a href="#">Fig. 18</a>	-	55	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 LPAK88 (SOT1235)	 mbb076
2	S	Source		
3	S	Source		
4	S	Source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R5-80SSE	LPAK88	plastic, single-ended surface-mounted package (LPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R5-80SSE	X2E5S80S

8. Limiting values

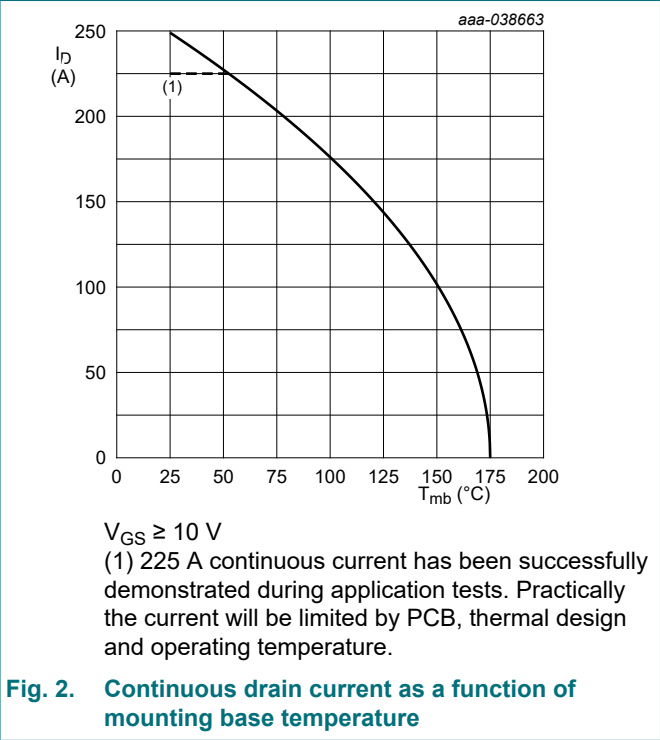
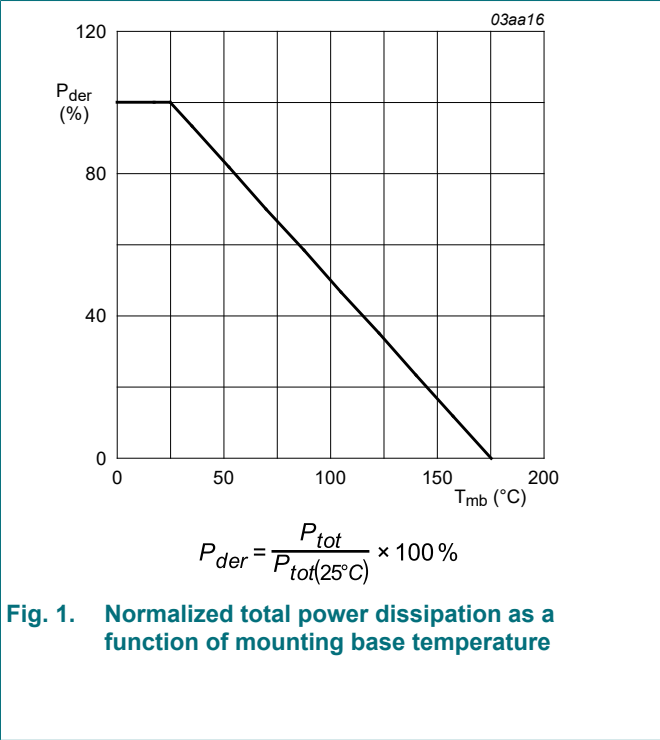
Table 5. Limiting values

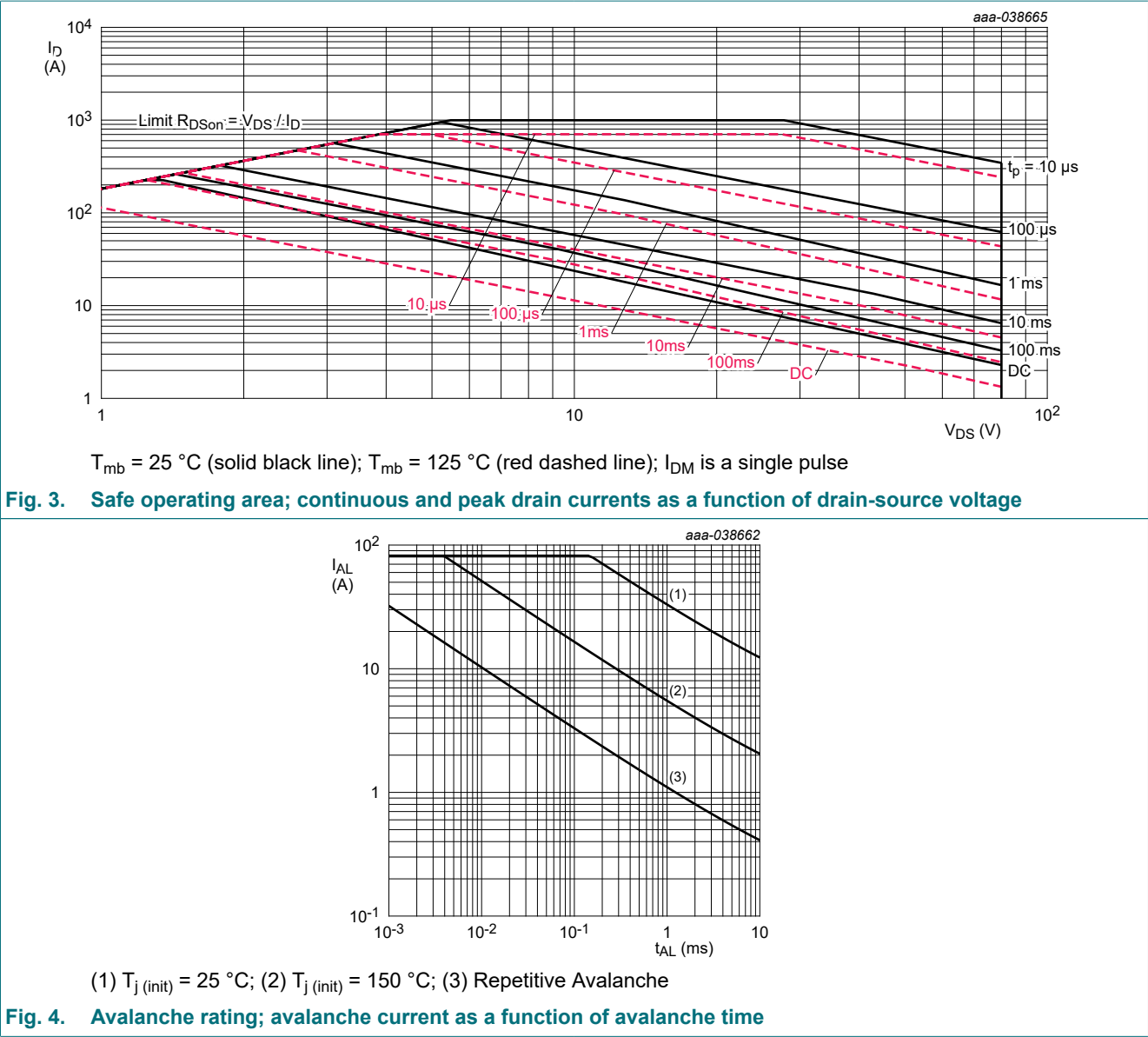
In accordance with the Absolute Maximum Rating System (IEC 60134). T<sub>j</sub> = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	80	V
V <sub>DGR</sub>	drain-gate voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ	-	80	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>	-	341	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>	-	225	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <a href="#">Fig. 2</a>	-	176	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 3</a>	-	996	A
T <sub>stg</sub>	storage temperature		-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>j</sub>	junction temperature			-55	175	°C
T <sub>sld(M)</sub>	peak soldering temperature			-	260	°C
Source-drain diode						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C		-	225	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	996	A
Avalanche ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 82 A; V <sub>sup</sub> ≤ 80 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; t <sub>p</sub> = 147 μs; <a href="#">Fig. 4</a>	[1]	-	628	mJ
I <sub>AS</sub>	non-repetitive avalanche current	V <sub>sup</sub> ≤ 80 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; R <sub>GS</sub> = 50 Ω; <a href="#">Fig. 4</a>	[1]	-	82	A

[1] Protected by 100% test





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	0.32	0.44	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	<a href="#">Fig. 6</a>	-	35	-	K/W
		<a href="#">Fig. 7</a>	-	70	-	K/W

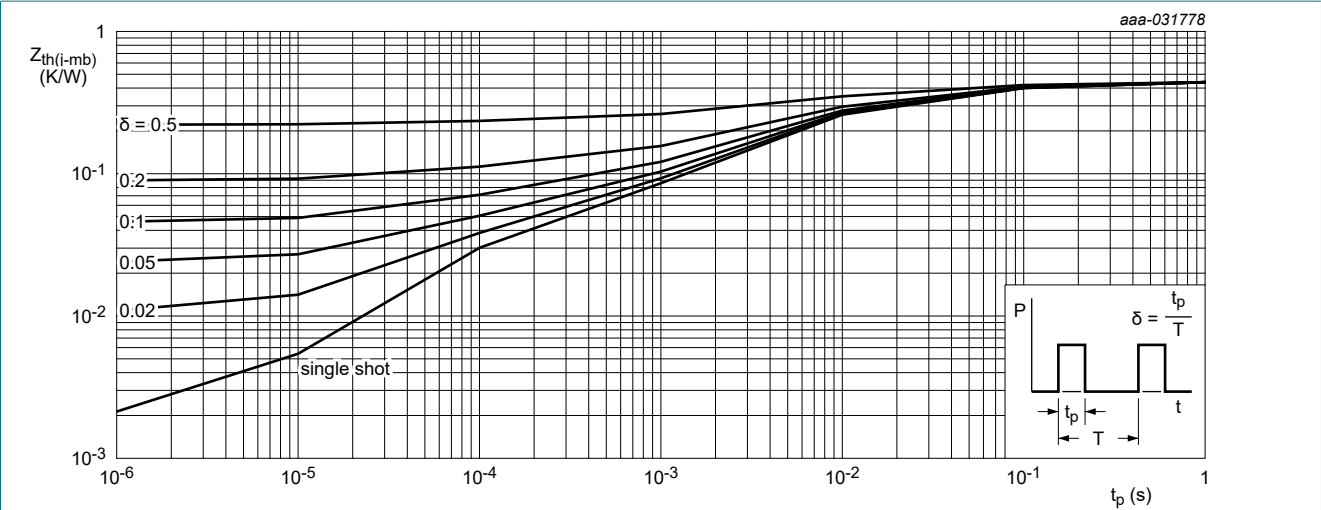
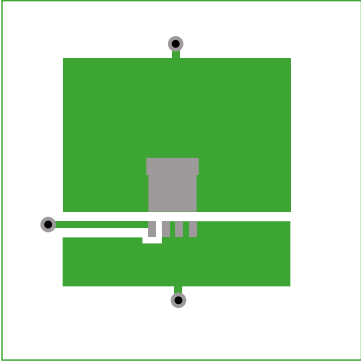


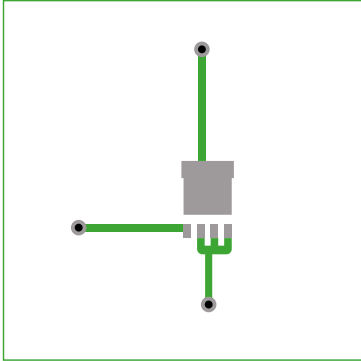
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration



aaa-029383

Copper square 25.4 mm square; 70 μm thick on FR4 board

Fig. 6. PCB layout for thermal resistance from junction to ambient



aaa-029384

70 μm thick copper on FR4 board

Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C	80	-	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = -55 °C	72	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>J</sub> = 25 °C; Fig. 11	2	2.6	3.6	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>J</sub> = 175 °C	-	1.6	-	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>J</sub> = -55 °C	-	3	-	V
ΔV <sub>GS(th)</sub> /ΔT	gate-source threshold voltage variation with temperature	25 °C ≤ T <sub>J</sub> ≤ 150 °C	-	-6.6	-	mV/K
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C	-	0.06	1	μA
		V <sub>DS</sub> = 80 V; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 125 °C	-	20	100	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>J</sub> = 25 °C	-	0.7	100	nA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>J</sub> = 25 °C	-	0.7	100	nA

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 25 °C; <a href="#">Fig. 12</a>		-	2	2.5	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 100 °C; <a href="#">Fig. 13</a>		-	2.9	3.8	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 175 °C; <a href="#">Fig. 13</a>		-	4.1	5.5	mΩ
R <sub>G</sub>	gate resistance	f = 1 MHz; T <sub>J</sub> = 25 °C		0.6	1.3	2.5	Ω
Dynamic characteristics							
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 10 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		58	116	174	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V; T <sub>J</sub> = 25 °C		-	108	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 10 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		27	45	63	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge			-	27	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge			-	18	-	nC
Q <sub>GD</sub>	gate-drain charge			4	13.4	31	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 40 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		-	4.9	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; f = 0.5 MHz; T <sub>J</sub> = 25 °C; <a href="#">Fig. 16</a>		5779	9632	13485	pF
C <sub>oss</sub>	output capacitance			1505	2509	4014	pF
C <sub>rss</sub>	reverse transfer capacitance			5	52	156	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 40 V; R <sub>L</sub> = 1.6 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 5 Ω; T <sub>J</sub> = 25 °C		-	36	-	ns
t <sub>r</sub>	rise time			-	32	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	59	-	ns
t <sub>f</sub>	fall time			-	43	-	ns
Source-drain diode							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 17</a>		-	0.8	1	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 40 V; <a href="#">Fig. 18</a>		-	51	-	ns
Q <sub>r</sub>	recovered charge			-	55	-	nC

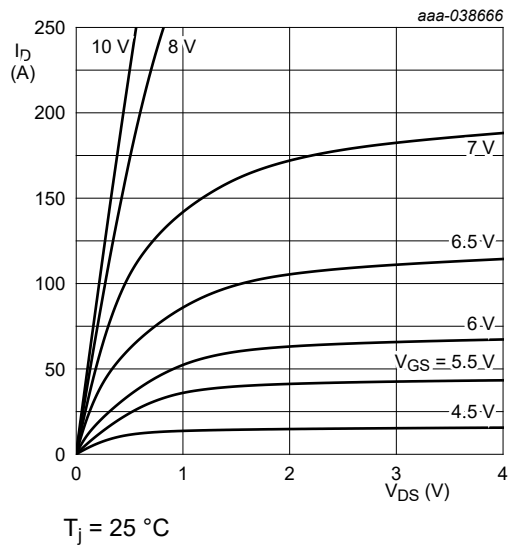


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

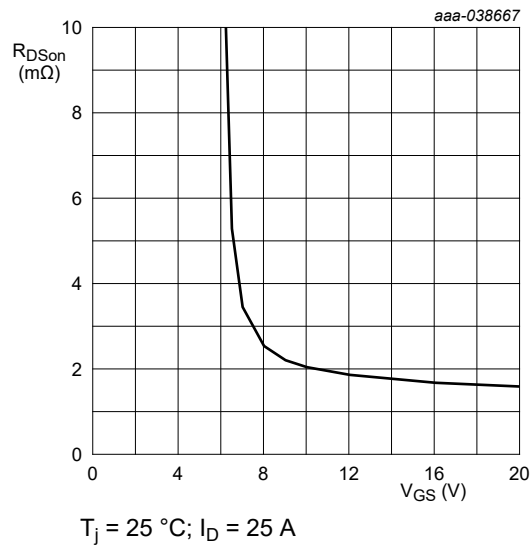


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

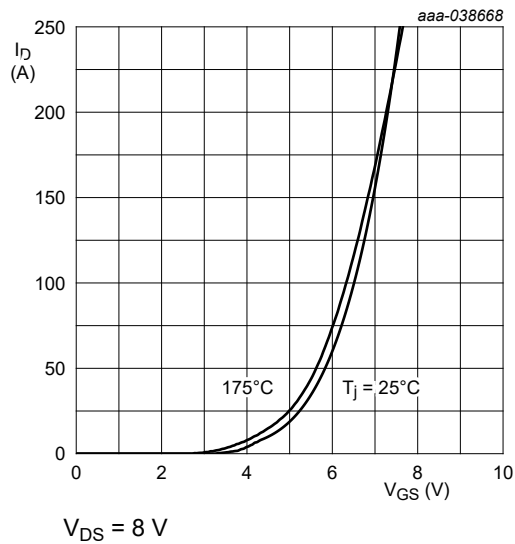


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

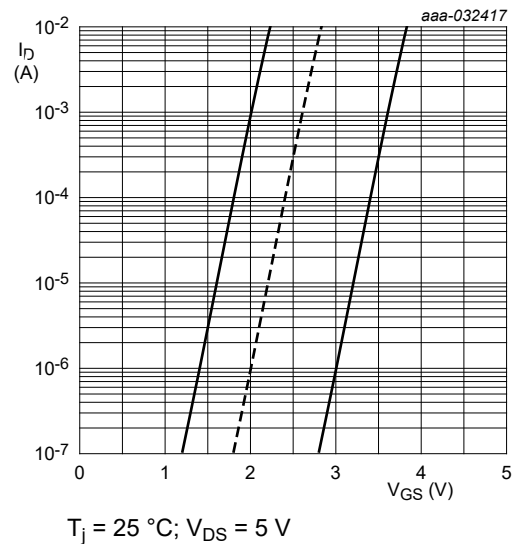


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

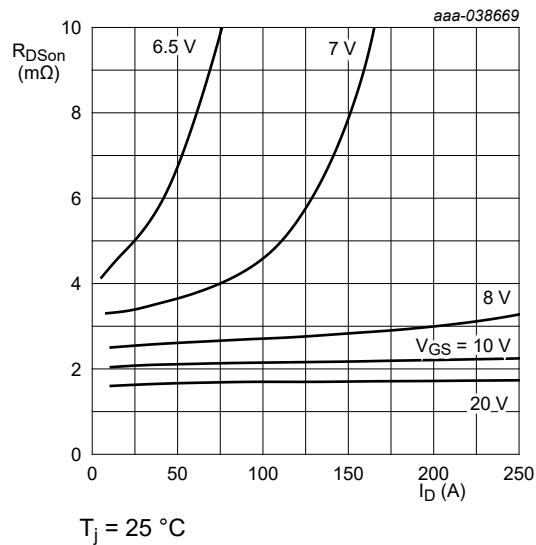


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

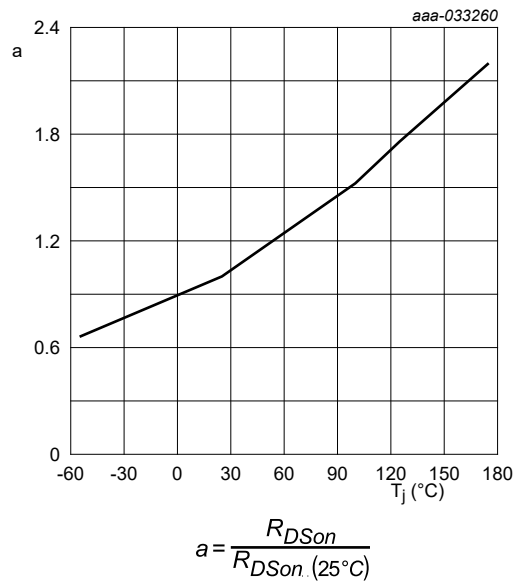


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

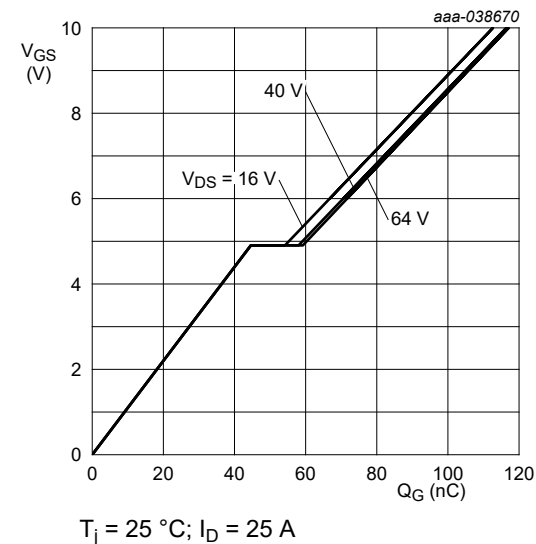


Fig. 14. Gate-source voltage as a function of gate charge; typical values

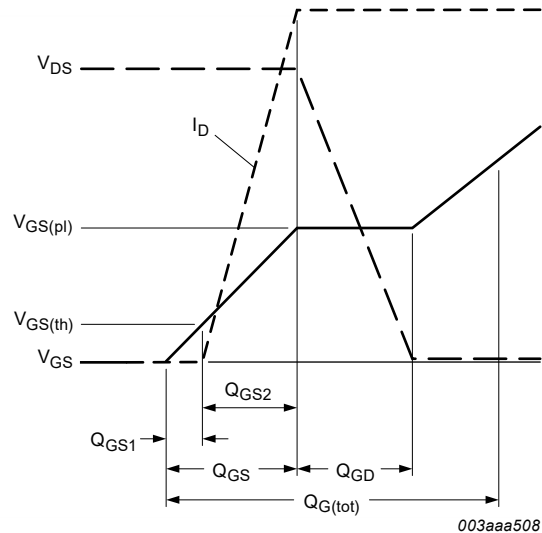


Fig. 15. Gate charge waveform definitions



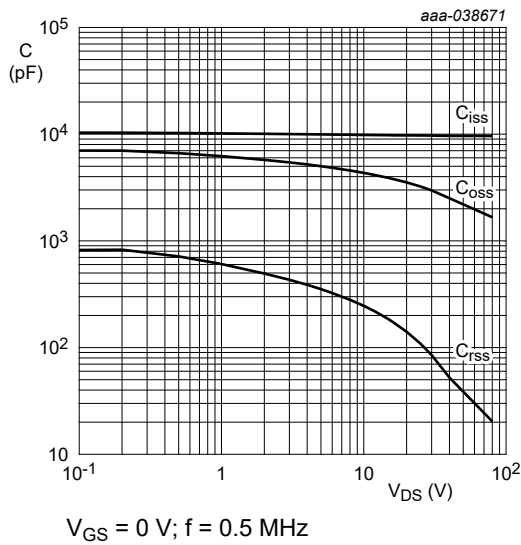


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

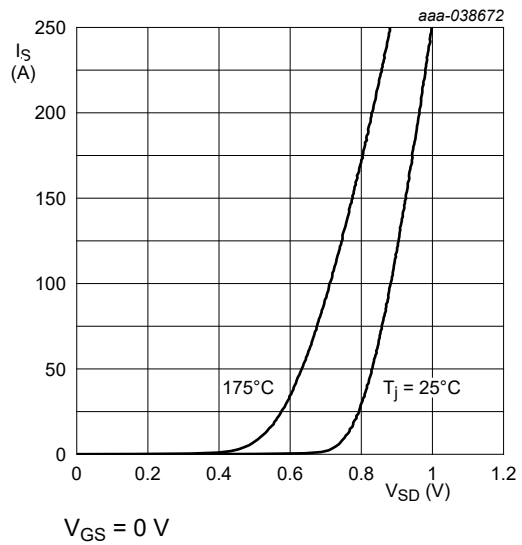


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

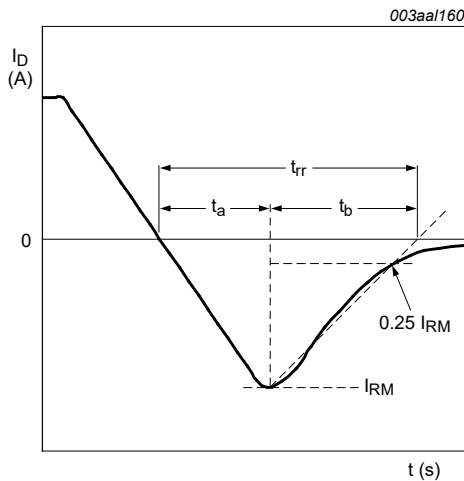


Fig. 18. Reverse recovery timing definition

11. Package outline

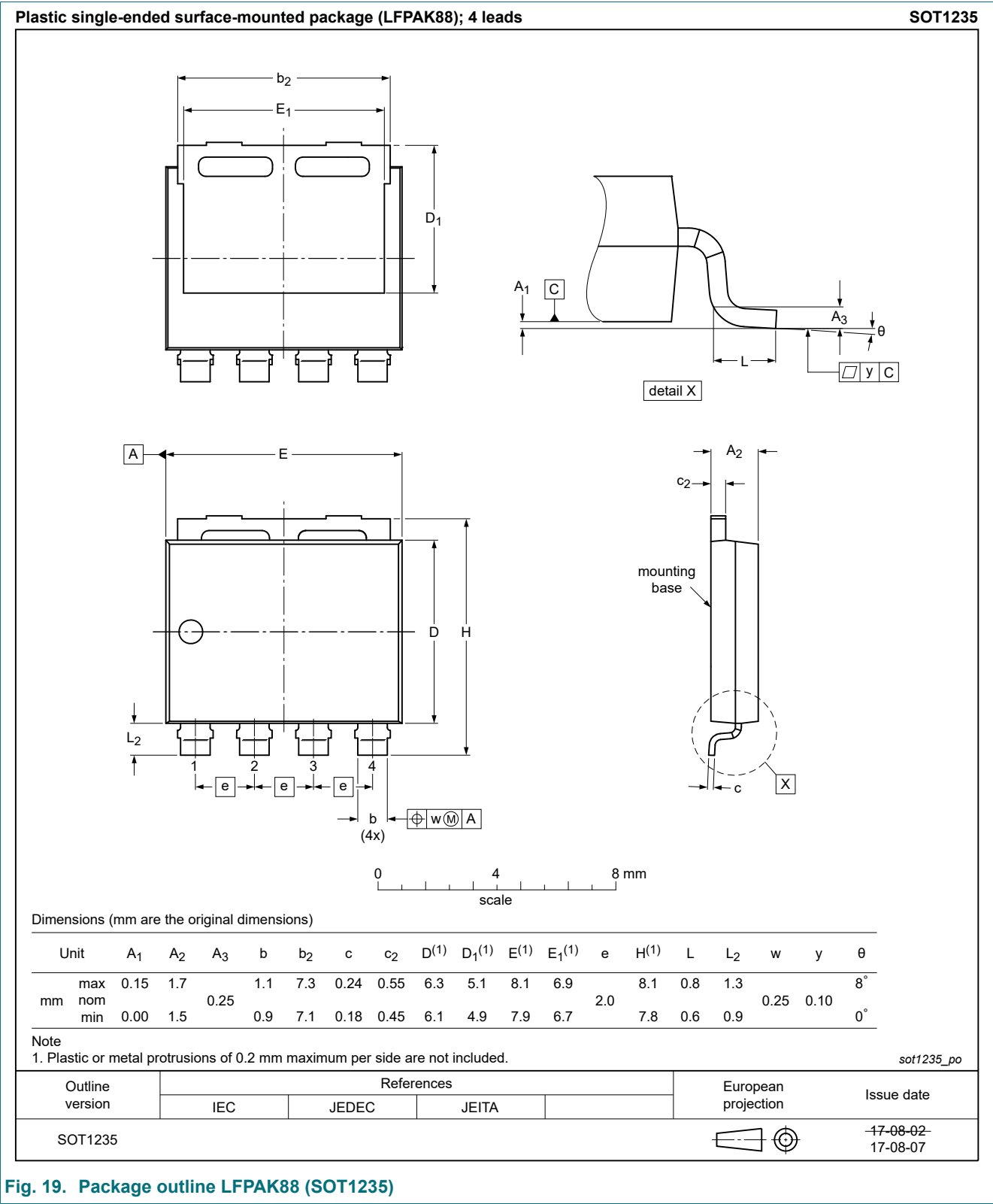
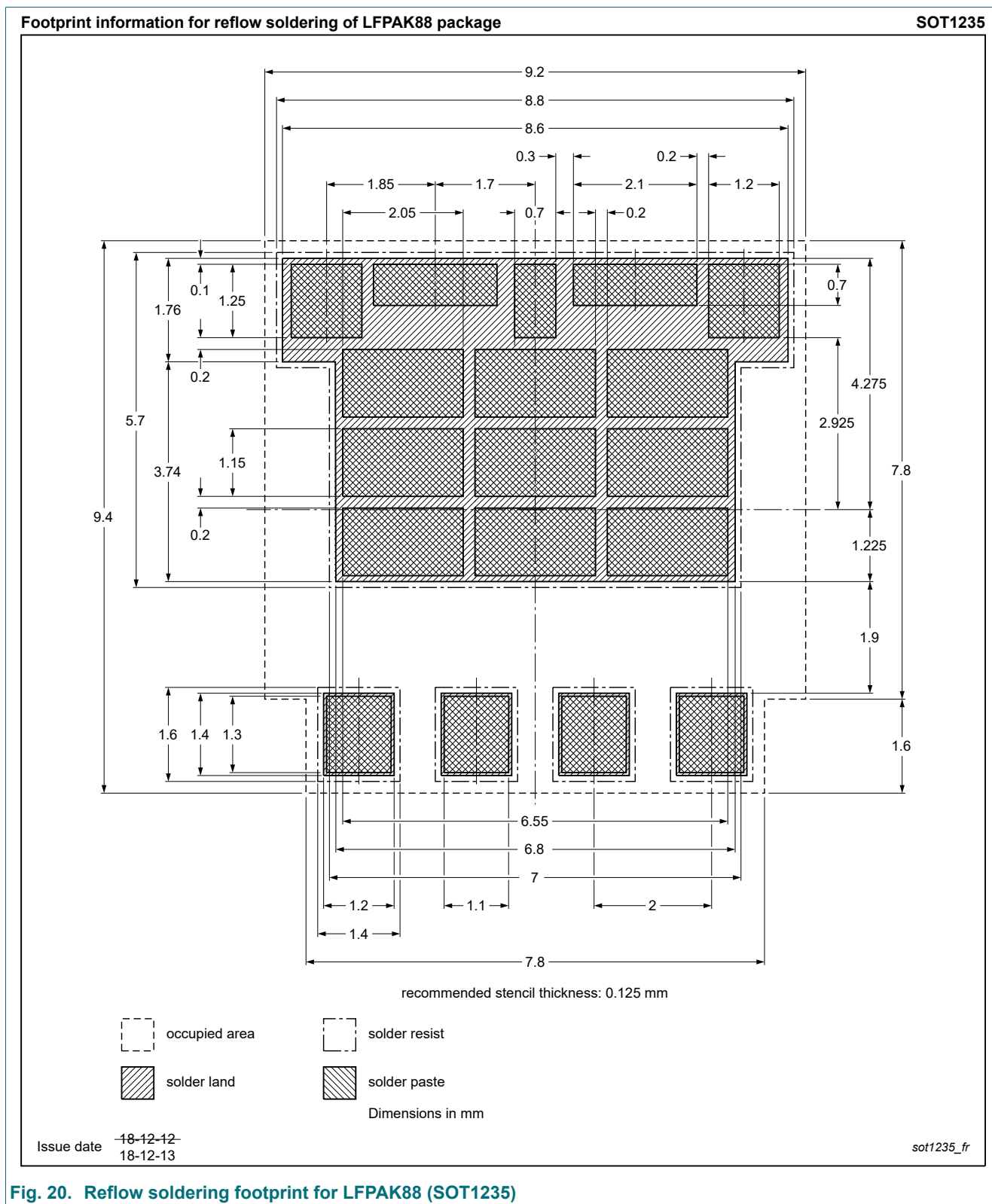


Fig. 19. Package outline LPAK88 (SOT1235)

## 12. Soldering



**Fig. 20. Reflow soldering footprint for LPAK88 (SOT1235)**

### 13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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