PSMNR70-40YSN

N-channel 40 V, 0.81 mOhm, 320 A standard level MOSFET in LFPAK56E using NextPower-S3 Schottky-Plus technology

27 February 2024 Preliminary data sheet

1. General description

320 Amp, standard level gate drive N-channel enhancement mode MOSFET in 175 °C LFPAK56E package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

2. Features and benefits

- 320 A continuous $I_{D(max)}$
- Avalanche rated, 100% tested at I_{AS} = 190 A
- Low spiking, allowing for high system efficiency and low EMI designs
- NextPower-S3 technology delivers 'superfast switching with soft body-diode recovery
- Low Q_{rr}, spiking, ringing, and oscillation for high system efficiency and low EMI designs
- Schottky-Plus body-diode with low V_{SD}, and low I_{DSS} leakage
- High reliability LFPAK (Power SO8) package, with copper-clip and solder die attach, qualified to 175 °C
- Exposed leads for enhanced visual solder joint inspection and high-quality solder joints for ultimate reliability
- Low parasitic inductance and resistance

3. Applications

- High-performance synchronous rectification
- DC-to-DC converters
- High performance and high efficiency server power supply
- Brushless DC motor control
- Battery protection
- Load-switch
- eFuse

4. Quick reference data

Table 1. Quick reference data

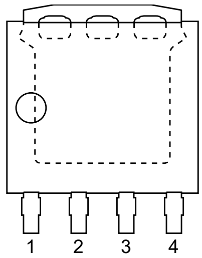
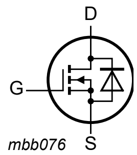
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	-	320	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	333	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12		0.48	0.68	0.81	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 125 °C; Fig. 13		0.71	1.06	1.33	mΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 14; Fig. 15		18	59	100	nC
$Q_{G(tot)}$	total gate charge			107	179	251	nC
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 80.75 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 304 μs; Fig. 4	[2]	-	-	638	mJ
Source-drain diode							
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/μs; V_{GS} = 0 V; V_{DS} = 20 V; Fig. 18	[3]	-	31	-	nC

[1] 320 A continuous current will be demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Protected by 100% test
[3] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK56E; Power-SO8 (SOT1023)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR70-40YSN	LFPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LFPAK56E); 4 leads; 1.27 mm pitch	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR70-40YSN	N9040S

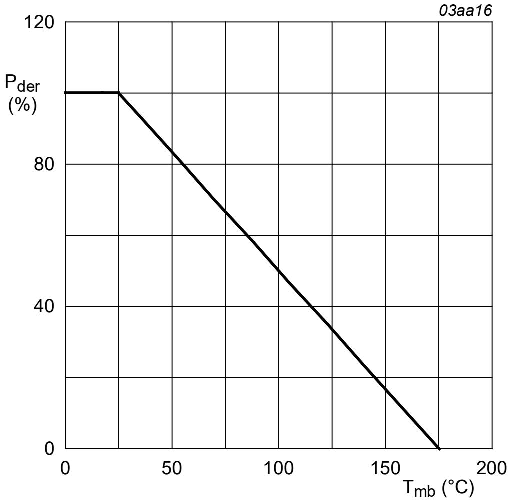
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).Tj = 25 °C unless otherwise stated.

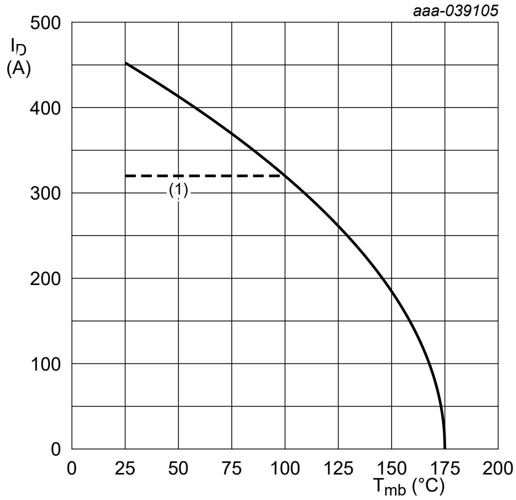
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	40	V
V_{DSM}	peak drain-source voltage	t_p = 20 ns; f = 500 kHz; $E_{DS(AL)}$ = 200 nJ; single pulse		-	45	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	333	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2	[1]	-	320	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	320	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	1810	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	320	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	1810	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 80.75 A; V_{sup} ≤ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 304 µs; Fig. 4	[2]	-	638	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} ≤ 40 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; Fig. 4	[2]	-	190	A

[1] 320 A continuous current will be demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Protected by 100% test



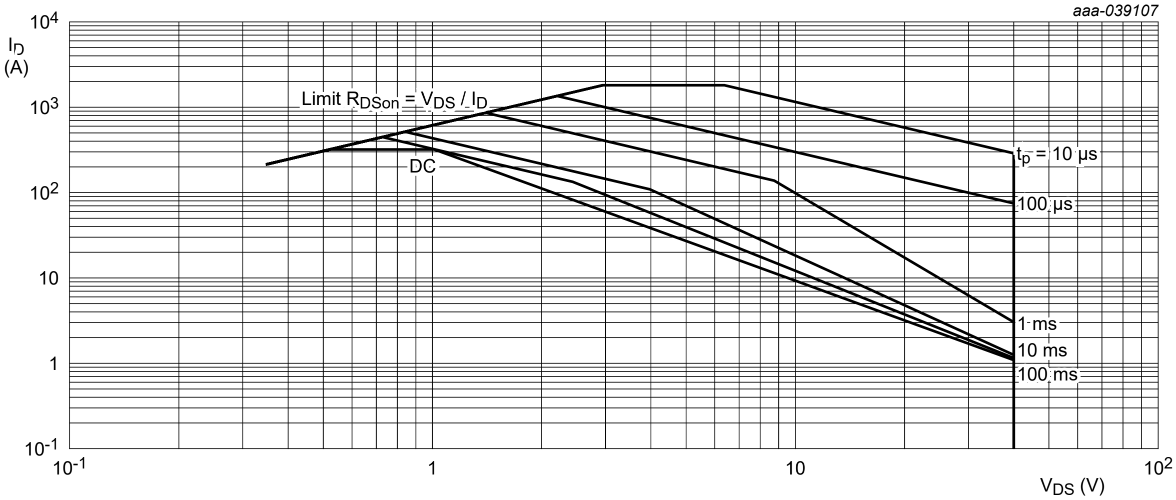
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



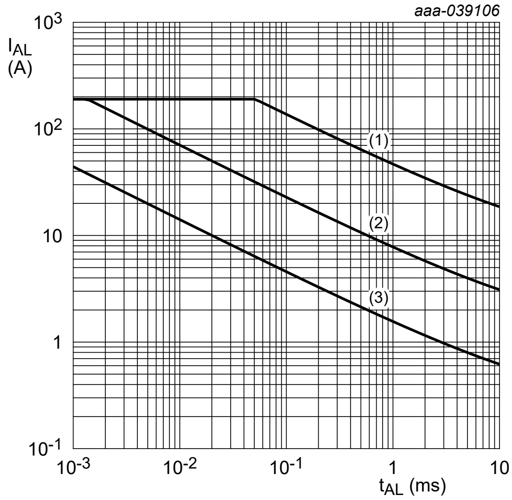
V_{GS} ≥ 10 V
(1) 320 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\ (init)}$ = 25 °C; (2) $T_{j\ (init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.4	0.45	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6		-	42	-	K/W
		Fig. 7		-	85	-	K/W

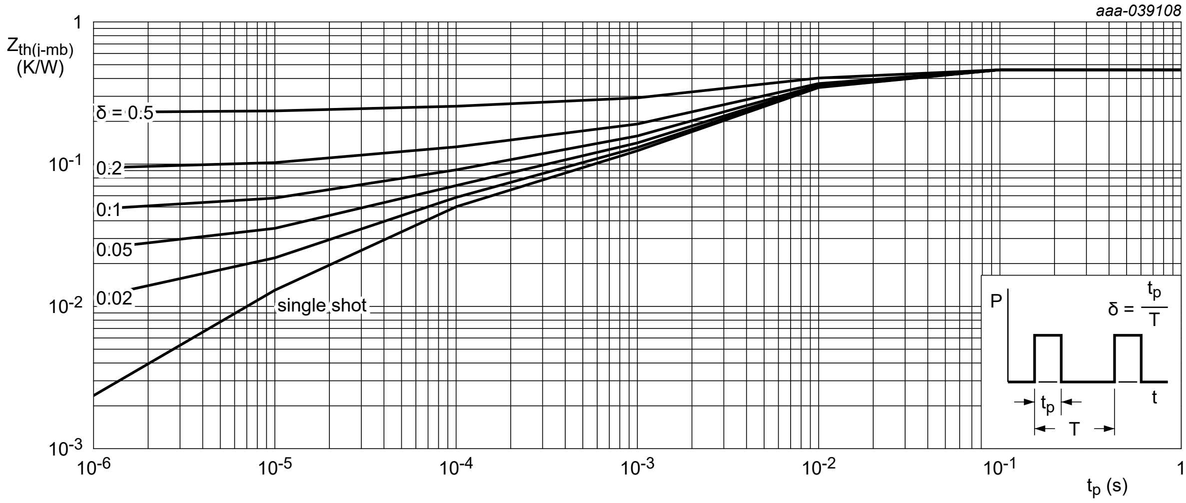


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

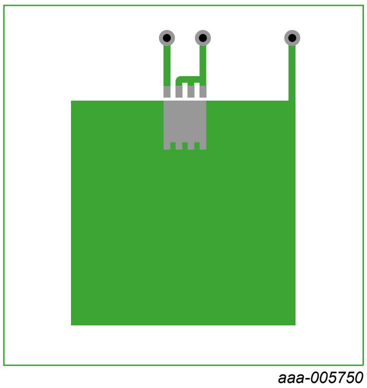


Fig. 6. PCB layout for thermal impedance junction to ambient 1" square pad; FR4 Board; 2oz copper

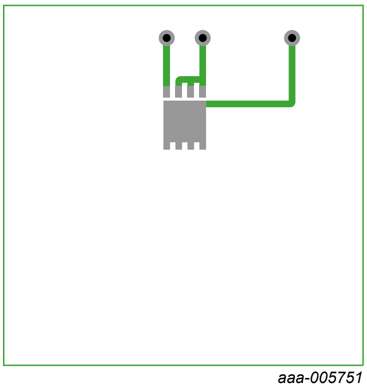


Fig. 7. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

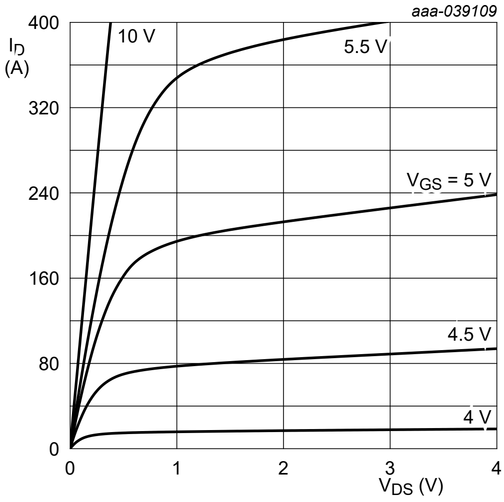
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 11		2.4	2.9	3.6	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	3.3	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C		-	1.8	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 175 °C		-	-7.7	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 32 V; V_{GS} = 0 V; T_j = 25 °C		-	0.3	1	µA
		V_{DS} = 16 V; V_{GS} = 0 V; T_j = 125 °C		-	1.5	10	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA

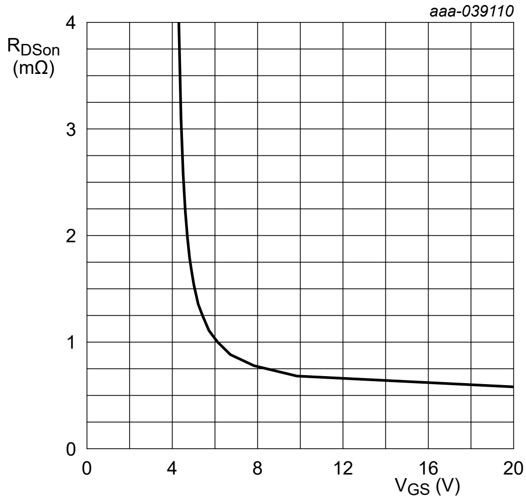
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 12		0.48	0.68	0.81	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 105 °C; Fig. 13		0.65	0.97	1.22	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 125 °C; Fig. 13		0.71	1.06	1.33	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 13		0.84	1.3	1.8	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		0.32	0.81	2.03	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 14; Fig. 15		107	179	251	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 14; Fig. 15		-	134	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; Fig. 14; Fig. 15		19	35	51	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	25	36	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	11	15	nC
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 14; Fig. 15		18	59	100	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 32 V; T_j = 25 °C; Fig. 14; Fig. 15		-	4.2	-	V
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 16		6040	10067	14094	pF
C_{oss}	output capacitance			1558	2226	2894	pF
C_{rss}	reverse transfer capacitance			353	883	1413	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω		-	30	-	ns
t_r	rise time			-	53	-	ns
$t_{d(off)}$	turn-off delay time			-	99	-	ns
t_f	fall time			-	70	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17		-	0.77	1	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; Fig. 18		-	38	-	ns
Q_r	recovered charge		[1]	-	31	-	nC

[1] includes capacitive recovery



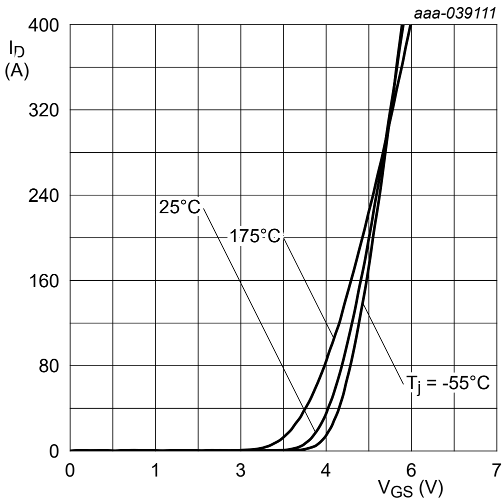
T_j = 25 °C

Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values



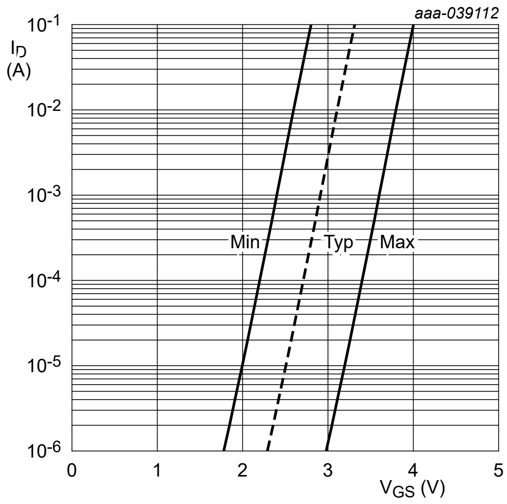
T_j = 25 °C; I_D = 25 A

Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



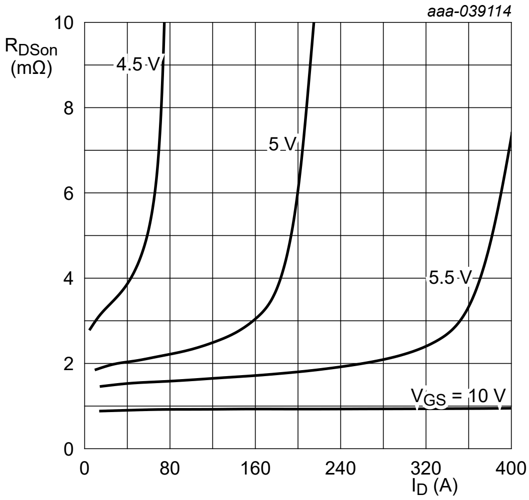
V_{DS} = 8 V

Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values



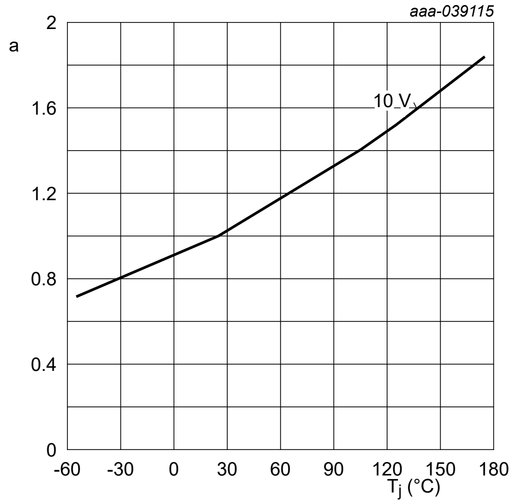
T_j = 25 °C; V_{DS} = 5 V

Fig. 11. Sub-threshold drain current as a function of gate-source voltage



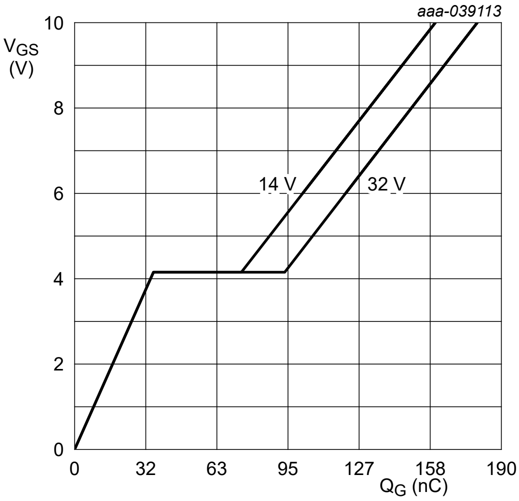
T_j = 25 °C

Fig. 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon\,(25°C)}}$$

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 25 A

Fig. 14. Gate-source voltage as a function of gate charge; typical values

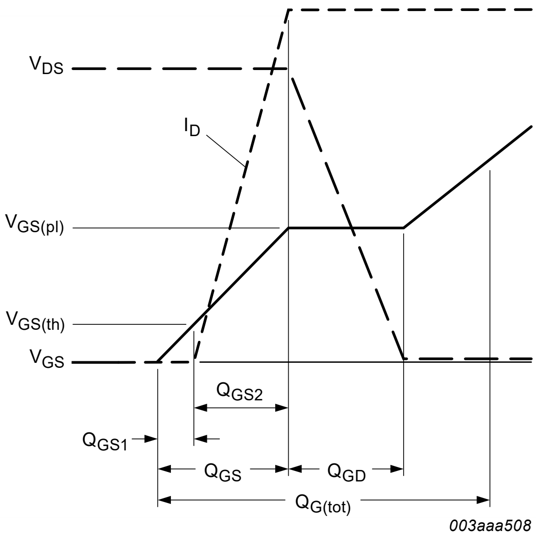
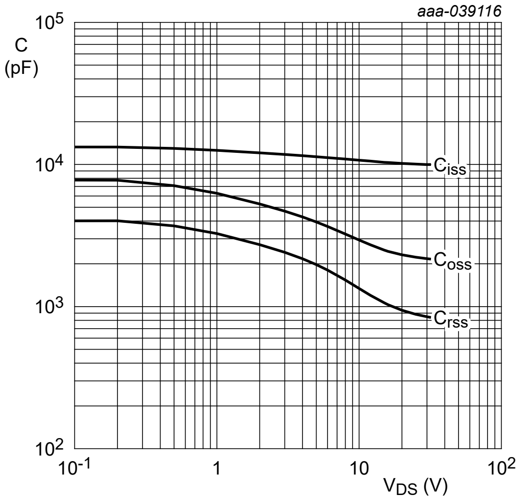
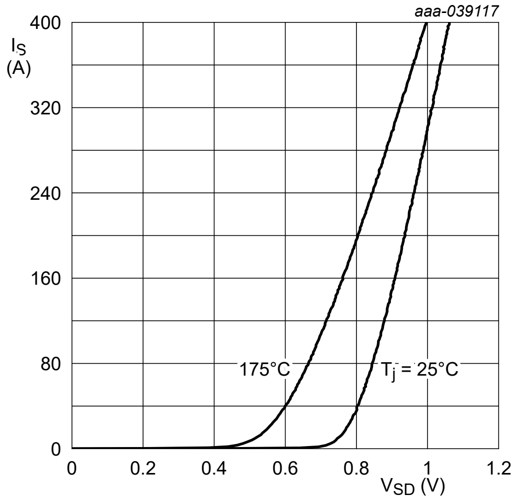


Fig. 15. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



V_{GS} = 0 V

Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

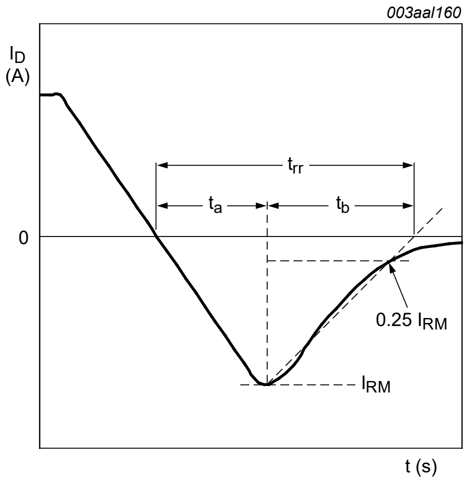
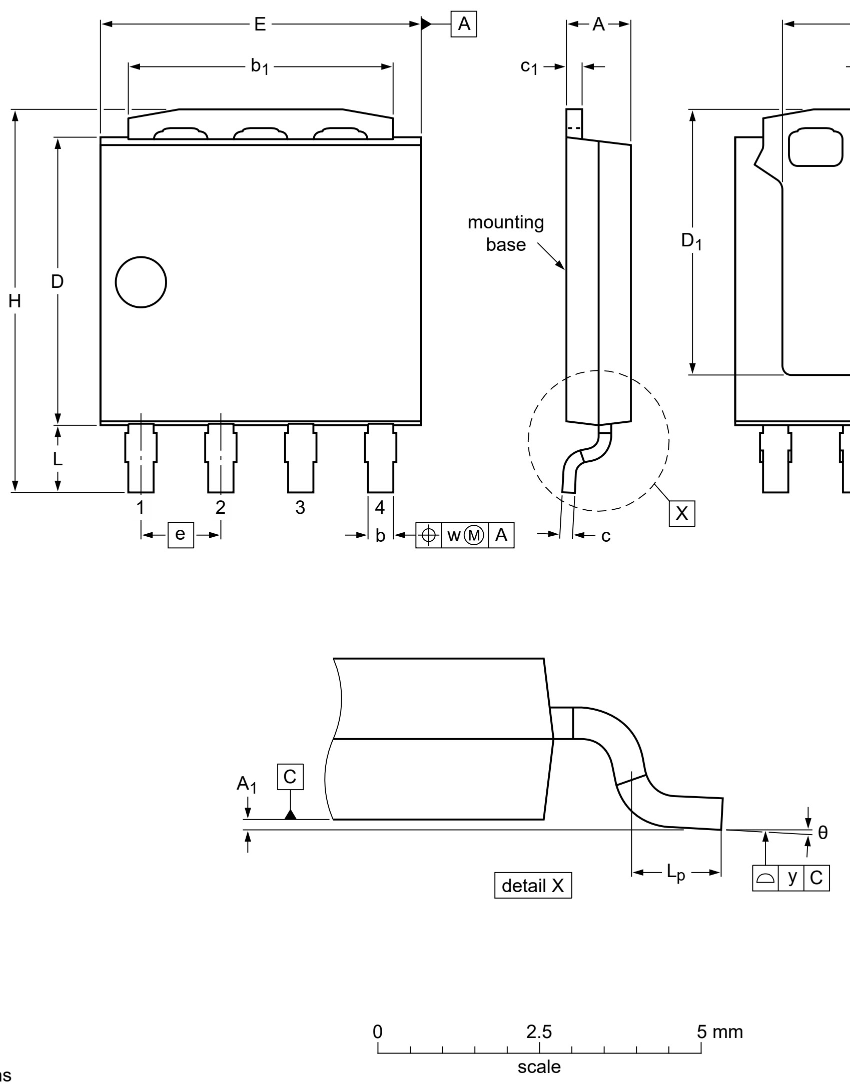


Fig. 18. Reverse recovery timing definition

11. Package outline

Plastic single-ended surface-mounted package (LFPAK56E); 4 leads **SOT1023**



Dimensions

Unit		A	A_1	b	b_1	b_2	c	c_1	D(1)	D_1(1)	E(1)	E_1(1)	e	H	L	L_p	w	y	θ
mm	max	1.10	0.15	0.50	4.41		0.25	0.30	4.70	4.45	5.30	3.7		6.2	1.3	0.85			8°
	nom					0.85							1.27				0.25	0.1	
	min	0.95	0.00	0.35	3.62		0.19	0.24	4.45		4.95	3.5		5.9	0.8	0.40			0°

Note
1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1023_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1023						~~13-03-05~~ 17-07-31

Fig. 19. Package outline LFPAK56E; Power-SO8 (SOT1023)

12. Soldering

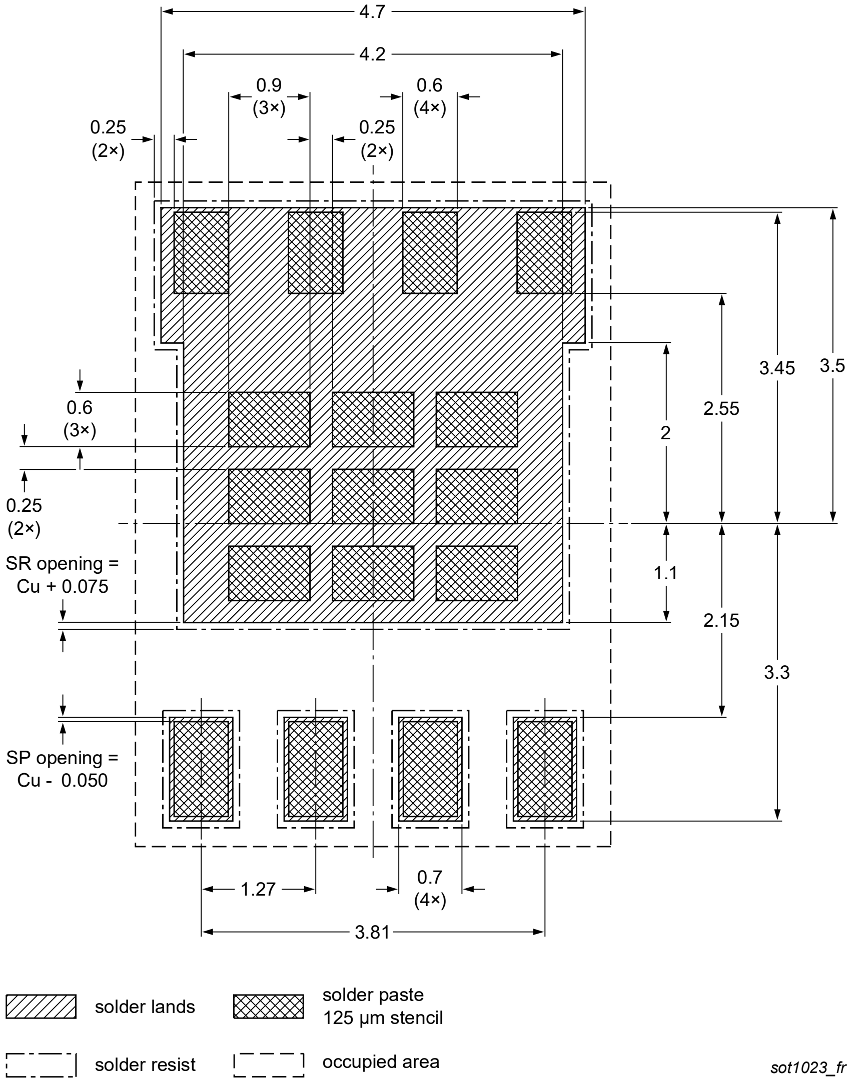


Fig. 20. Reflow soldering footprint for LFPAK56E; Power-SO8 (SOT1023)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 27 February 2024