I²C GPIO Expanders

Increase system flexibility and reusability in the system design

I²C GPIO expanders offer a solution to the challenges faced by system engineers in integrating next-generation technologies with legacy sub-systems. The use of a common bus for communication between different sub-systems and peripherals allows for a modular and flexible design that can be reused for multiple purposes. The expanders provide additional GPIOs, solving the problem of limited GPIOs and enabling the integration of advanced and legacy peripheral devices. By using I²C GPIO expanders, system engineers can maximize system reuse and integration of new feature sets, thereby meeting the demands of consumers and staying ahead in a rapidly evolving technology landscape.

The newest I²C GPIO expander portfolio offered by Nexperia provides excellent performance in pin-to-pin compatible packages with industry-standard footprints. The use of the I²C interface standard, which is a shared bus based on a controller and target protocol, reduces board routing complexity and minimizes manufacturing costs. The I²C bus can be routed throughout the system, which helps in reducing the number of board layers and maximizing system reuse. The advantage of I²C is its ability to support multiple nodes, which increases system flexibility and allows for the integration of new peripherals and feature sets. Overall, the I²C GPIO expanders from Nexperia offer a cost-effective and flexible solution for expanding the number of GPIOs in a system.

Applications

- Servers, Routers
- Hardware control monitors,
- Gaming consoles
- TV & Monitors
- IOTs, Battery powered applications
- Automotive applications like ADAS, BCM, VCU, DCU, Car radio, Instrument cluster
- Medical devices using sensors
- Controlling and monitoring digital outputs such as LEDs and relays
- Reading digital inputs such as switches and sensors
- Interfacing with other I²C devices in the system, such as displays and sensors
- Implementing a multi-master I²C bus for increased system complexity and functionality.

nexperia

Features	Benefits
I²C bus to parallel port expander	Eliminates expensive congested PCB since a trace or wire is not needed for each signal.
Single supply GPIO expander supporting 1.65V to 5.5V operation	Lowers I/O usage & reduces the system BOM and manufacturing cost
Serial to parallel (SDA to P0-P16) and parallel to serial (P0-P16) conversion with I²C protocol	Board-space and Processor-pin saving
Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs	In case of migrating to more advance core processor, the processor's IO voltage may be connected to a single voltage domain
Low power consumption 2.5uA max	Eases choice to add or remove peripheral devices based on the target feature set adding to scalability
400kHz operation (FM I2C mode)	50ns spike filter allows further usage in noisy server environment providing robust solution
Glitch free Power up with all channels configured as inputs with Pull-ups	Lower propagation delay than the competition enabling fast response from I²C signals to GPIO signals
Latched outputs with 25 mA drive maximum capability for directly driving LEDs	Supports maximal system reuse
Support Polarity Inversion Register and Interrupt feature	Supports usage of multiple NCA9555 on the same bus
External RESET pin to reset state machine and internal registers	Low latency can be achieved using RESET feature
Noise filters on SCL and SDA inputs	Supports multiple NCA9555 I²C GPIO on the same Bus
Specified from -40 °C to +85 °C and -40 °C to +125 °C	

Block diagram – NCA9555

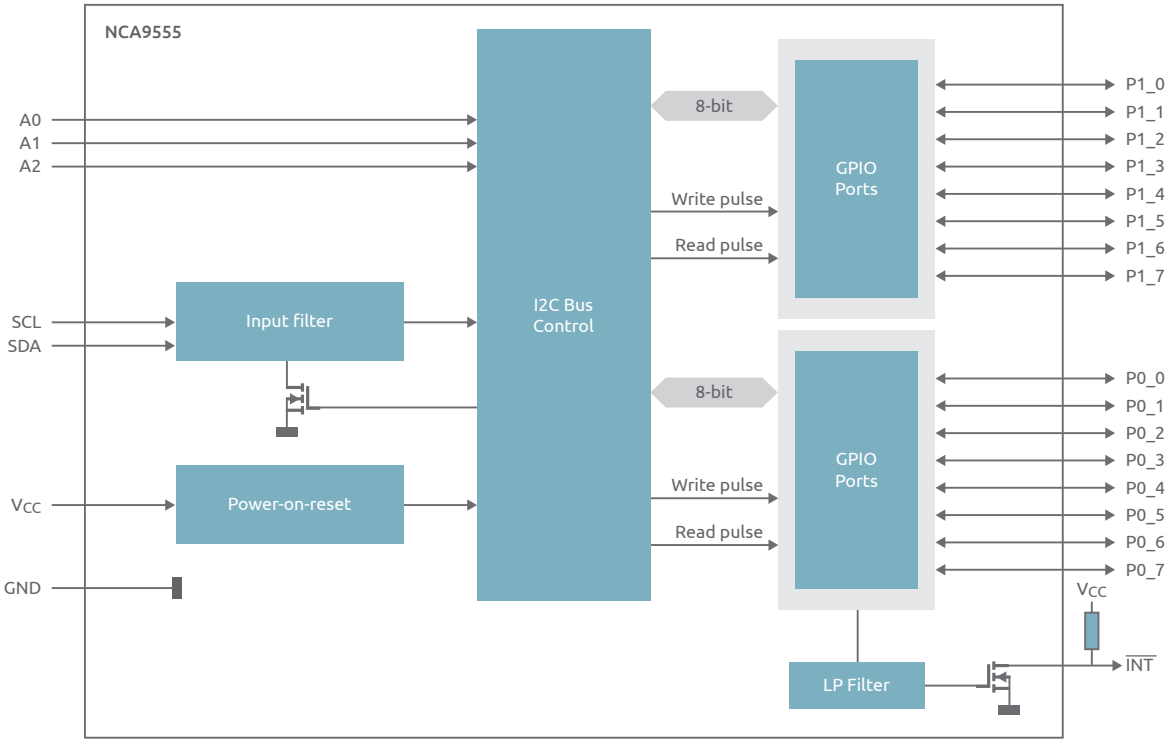
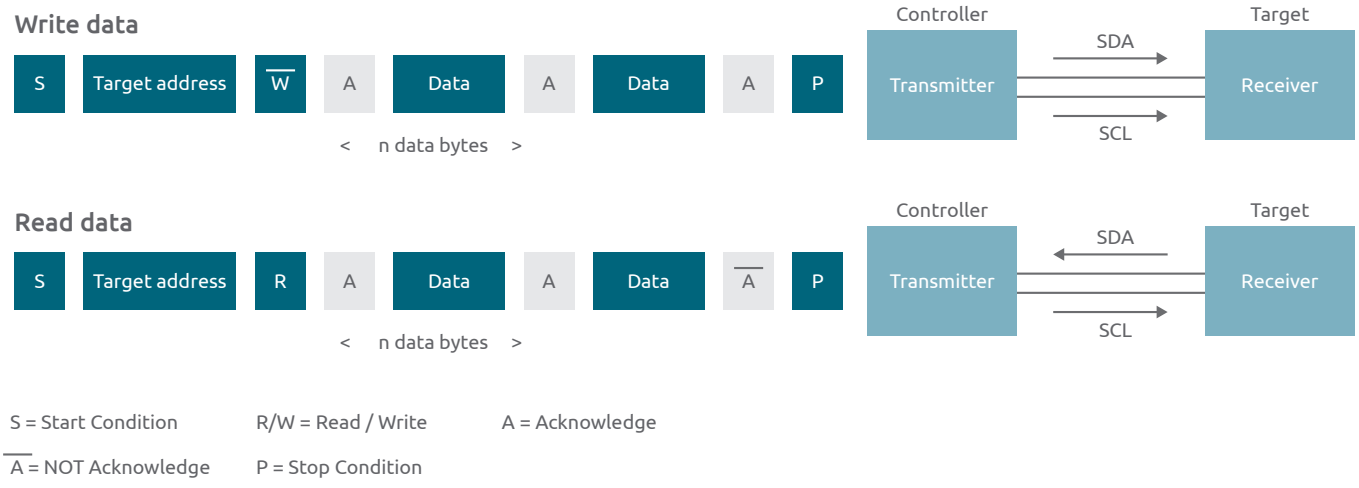


Figure 1: NCA9555 block diagram

Reading and writing to port registers

I²C bus devices are available in a wide range of functions. Each target device has its own I²C bus address, selectable using address pins set high (1) or low (0). Information is transmitted byte by byte, and each byte is acknowledged by the receiver. There can be multiple devices on the same bus, and more than one IC can act as controller. The controller role is typically played by a microcontroller.

The NCA9555 is an I²C bus target device. Data is exchanged between the controller and NCA9555 through write and read commands using I²C bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.



S = Start Condition R/W = Read / Write A = Acknowledge

$\overline{A}$ = NOT Acknowledge P = Stop Condition

Figure 2 : Read and write to ports

Writing to the port registers

Data is transmitted to the NCA9555 by sending the device address and setting the read-write bit to a logic 0.
The command byte is sent after the address and determines which register will receive the data following the command byte. Eight registers within the NCA9555 are configured to operate as four register pairs. The four pairs are input port, output port, polarity inversion, configuration registers.

After sending data to one register, the next data byte is sent to the other register in the pair. For example, if the first byte is sent to Output Port 0 (register 2), the next byte is stored in Output Port 1 (register 3). There is no limitation on the number of data bytes sent in one write transmission. In this way, the host can continuously update a register pair independently of the other registers, or the host can simply update a single register.

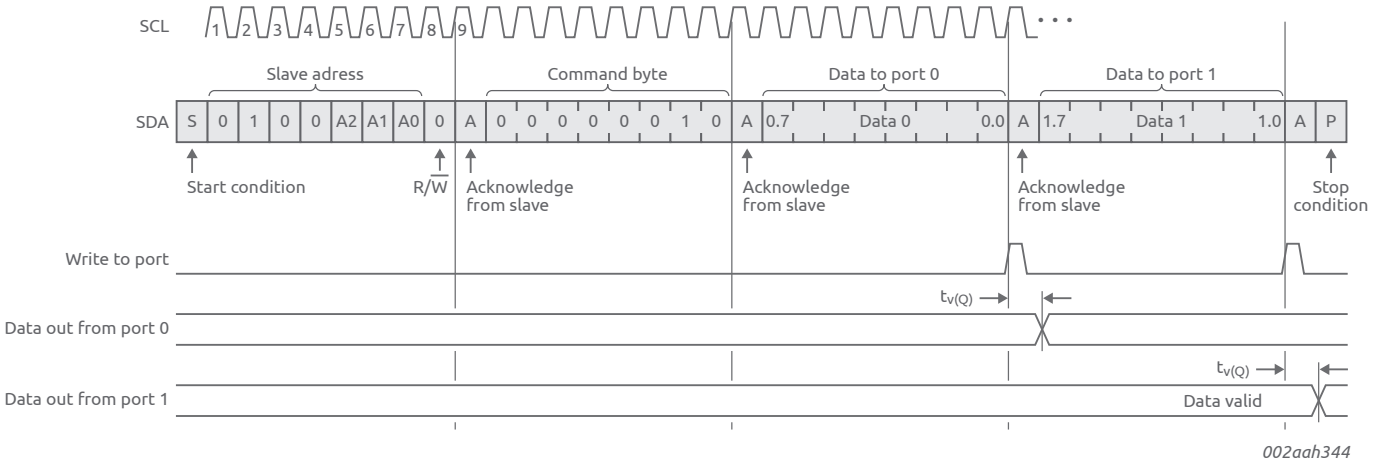


Figure 3 : Write to control registers

Reading the port registers

In order to read data from the NCA9555, the bus master must first send the NCA9555 address with the least significant bit set to a logic 0. The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte is sent by the NCA9555. Data is clocked into the register on the rising edge of the acknowledge clock pulse.

After the first byte is read, additional bytes may be read but the data now reflects the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0. There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data. After a subsequent restart, the command byte contains the value of the next register to be read in the pair. For example, if Input Port 1 was read last before the restart, the register that is read after the restart is the Input Port 0.

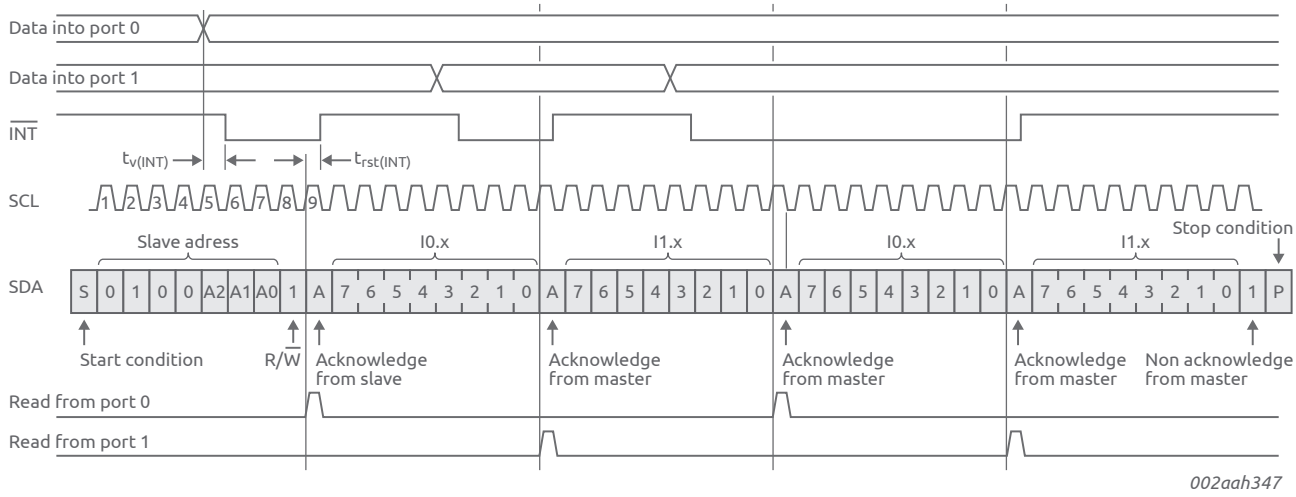
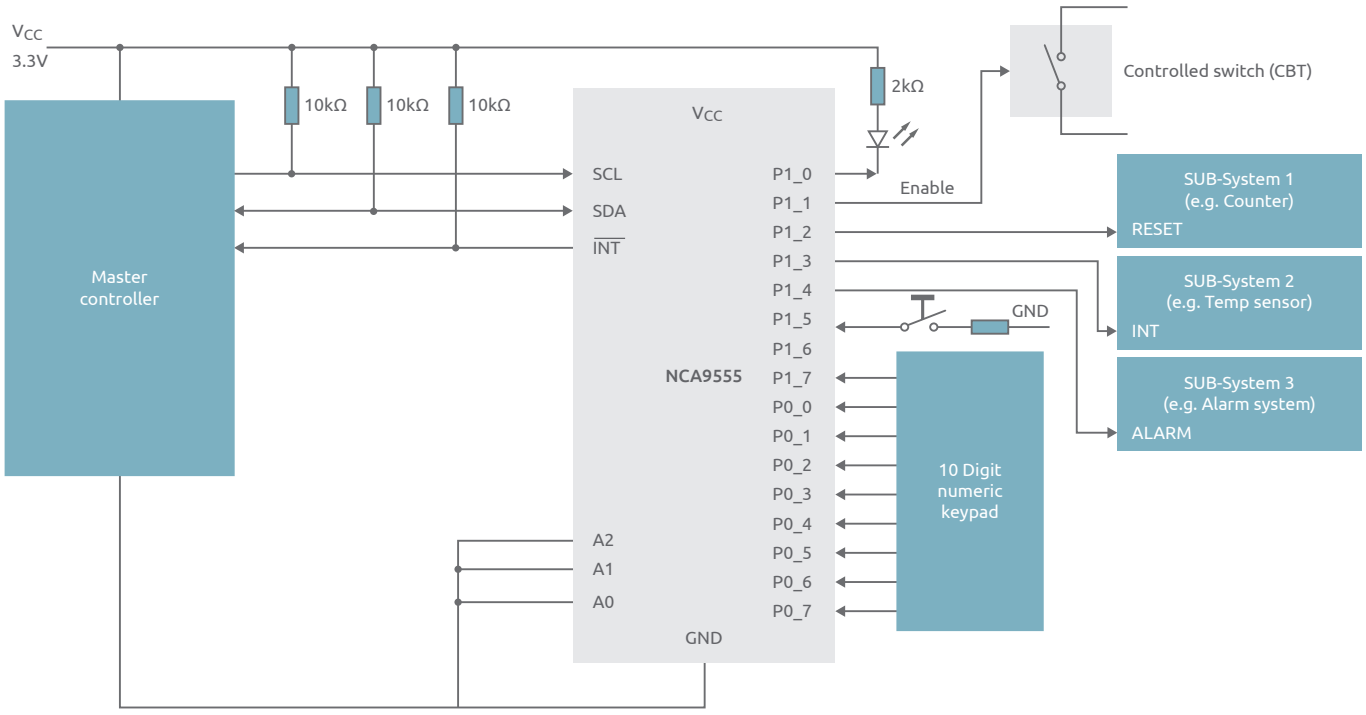


Figure 4 : Read from register

Application design-in information



P0_0, P0_2, P0_3 configured as outputs.
P0_1, P0_4, P0_5 configured as inputs.
P0_6, P0_7 and (P1_0 to P1_7) configured as inputs.
(1) Internal pull-up may be used to eliminate external components.

Figure : 5 Typical Application

When the I/Os are used to control LEDs, they are normally connected to VCC through a resistor. Since the LED acts as a diode, when the LED is off the I/O VI is about 1.2 V less than VCC. The supply current, ICC, increases as VI becomes lower than VCC.

Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to VCC when the LED is off. Fig. 7 shows VCC less than the LED supply voltage by at least 1.2 V. Both methods maintain the I/O VI at or above VCC and prevents additional supply current consumption when the LED is off.

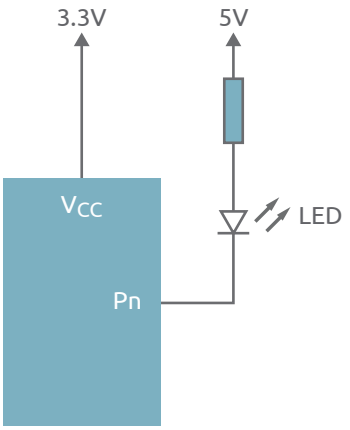
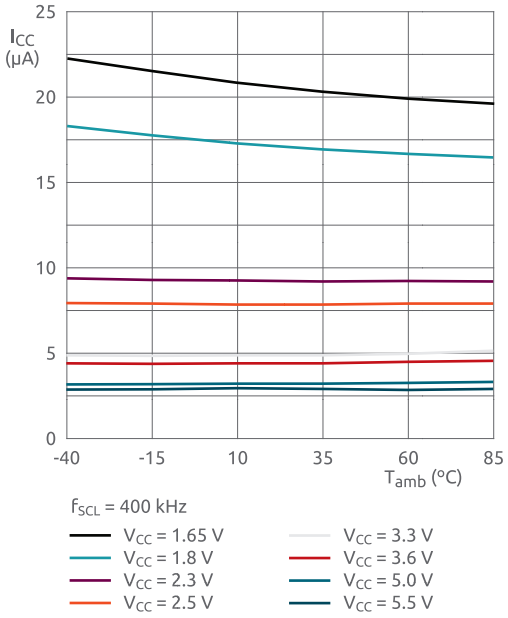
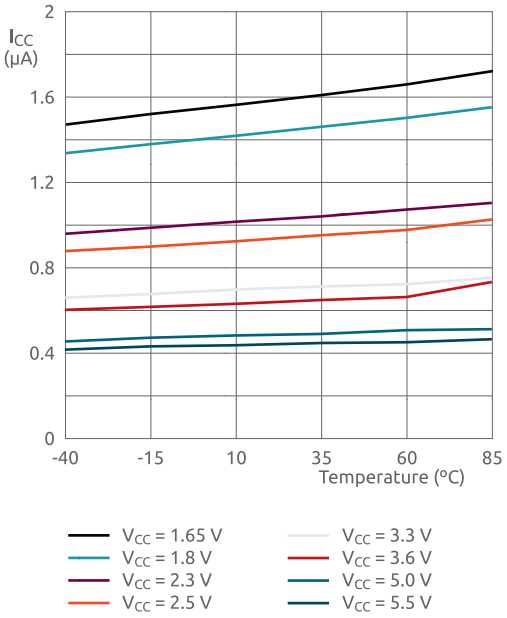


Figure 7: Device supplied by a lower voltage

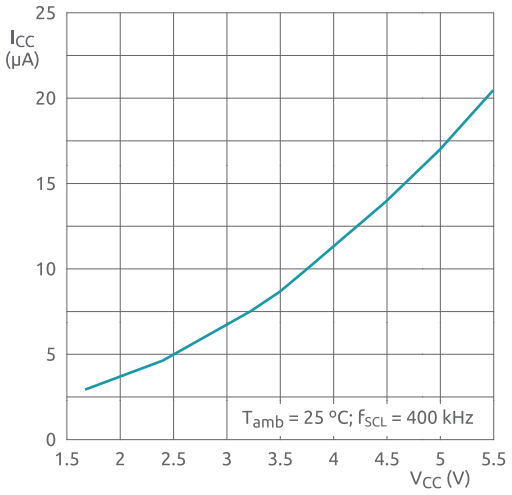
Typical charactertics



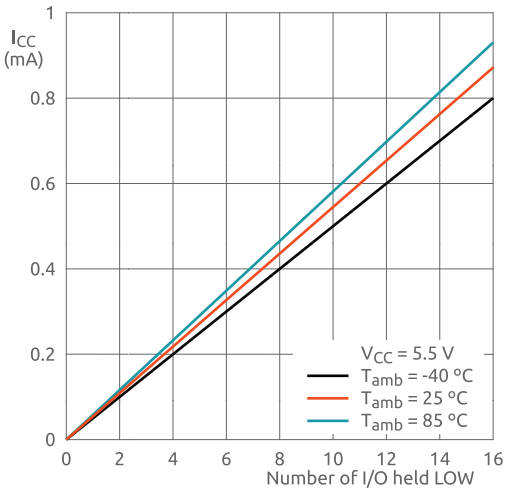
Supply current versus ambient temperature



Standby supply current versus ambient temperature



Supply current versus supply voltage



Supply current versus number of I/O held LOW

Product Portfolio

Family	Description	VCC (V)	Tamb (°C)	Nr of pins	Package name
NCA9555PW	Low-voltage 16-bit I²C and SMBus I/O expander with interrupt output and configuration registers	1.65 - 5.5	-40~85	24	TSSOP24
NCA9555BY	Low-voltage 16-bit I²C and SMBus I/O expander with interrupt output and configuration registers	1.65 - 5.5	-40~85	24	HWQFN24
NCA9539PW	Low-voltage 16-bit I²C and SMBus low-power I/O expander with interrupt output, reset pin and configuration registers	1.65 - 5.5	-40~85	24	TSSOP24
NCA9539BY*	Low-voltage 16-bit I²C and SMBus low-power I/O expander with interrupt output, reset pin and configuration registers	1.65 - 5.5	-40~85	24	HWQFN24
NCA9535PW	Low-voltage 16-bit I²C and SMBus low-power I/O expander with interrupt output and configuration registers	1.65 - 5.5	-40~85	24	TSSOP24
NCA9535BY*	Low-voltage 16-bit I²C and SMBus low-power I/O expander with interrupt output and configuration registers	1.65 - 5.5	-40~85	24	HWQFN24
NCA9595PW	Low voltage 16-bit I²C and SMBus I/O expander with interrupt output, configuration registers and programmable pull-up resistors	1.65 - 5.5	-40~85	24	TSSOP24
PCA9555PW	Low-voltage 16-bit I²C-bus I/O port with interrupt and weak pull-up	2.3 - 5.5	-40~85	24	TSSOP24
PCA9539PW	Low-voltage 16-bit I²C and SMBus low-power I/O expander with interrupt output, reset pin and configuration registers	2.3 - 5.5	-40~85	24	TSSOP24
PCA9535PW	Low-voltage 16-bit I²C and SMBus low-power I/O expander with interrupt output and configuration registers	2.3 - 5.5	-40~85	24	TSSOP24
NCA9595PW-Q100	Low voltage 16-bit I²C and SMBus I/O expander with interrupt output, configuration registers and programmable pull-up resistors	1.65 - 5.5	-40~125	24	TSSOP24
NCA9555PW-Q100	Low-voltage 16-bit I²C and SMBus I/O expander with interrupt output and configuration registers	1.65 - 5.5	-40~125	24	TSSOP24
NCA9555BY-Q100	Low-voltage 16-bit I²C and SMBus I/O expander with interrupt output and configuration registers	1.65 - 5.5	-40~125	24	HWQFN24
NCA9539PW-Q100	Low-voltage 16-bit I²C and SMBus low-power I/O expander with interrupt output, reset pin and configuration registers	1.65 - 5.5	-40~125	24	TSSOP24
NCA9539BY-Q100*	Low-voltage 16-bit I²C and SMBus low-power I/O expander with interrupt output, reset pin and configuration registers	1.65 - 5.5	-40~125	24	HWQFN24
NCA9535PW-Q100	Low-voltage 16-bit I²C and SMBus low-power I/O expander with interrupt output and configuration registers	1.65 - 5.5	-40~125	24	TSSOP24
NCA9535BY-Q100*	Low-voltage 16-bit I²C and SMBus low-power I/O expander with interrupt output and configuration registers	1.65 - 5.5	-40~125	24	HWQFN24

* in development

SOT	Package suffix	No of pins	Package dimensions	Pitch (mm)	Package
SOT355-1	PW	24	7.8 x 4.4 x 1.1	0.65	TSSOP24
SOT8041	BY	24	4 x 4 x 0.75	0.5	HWQFN24

Date of release:
April 2023