UM90026

Rev. 2 — 30 April 2024

user manual

NMUX1308; NMUX1309 evaluation board

Abstract: This user manual describes the NMUX1308; NMUX1309 evaluation board module.

Keywords: NMUX1308; NMUX1309 evaluation board

nexperia

1. Introduction

The NMUX1308; NMUX1309 EVB (Evaluation Board) is a PCB designed for Nexperia's CMOS, bi-directional, analog switches. The NMUX1308 device is an 8-channel analog switch, while the NMUX1309 incorporates dual 4 channel analog switches. The device features a wide voltage range of 1.5 V to 5.5 V. Additionally, the NMUX130x devices supports lower core voltages and is compatible with 1.8 V CMOS logic levels.

The NMUX1308 architecture is a single-pole eight-throw, (SP8T) analog switch, which enables multiplexed use to connect eight independent channels (Yn) to one common channel (Z). The channels can be individually selected through the control input pins.

The NMUX1309 features dual single-pole quadruple-throw, (SP4T), (4:1) analog switches. In each block, the four channels, (1Yn, 2Yn), can be configured to connect to its respective common channel, (nZ). This is accomplished by programming the control input pins.

All analog signals include integrated injection control circuitry. The control circuitry redirects any overvoltage or transient events on unselected pins and provides a controlled path to ground. This circuitry prevents the coupling of transients, therefore preserving measurement accuracy.

The EVB arrives enclosed in an antistatic ESD bag with labeling. The board provides two sets of silkscreen colors, allowing an easy way to reference either the NMUX1308 or NMUX1309 pin names. Convenient test points for GND, V_{CC}, Yn (1Yn, 2Yn), Z (nZ), Sn and enable ($\overline{E}$) pins are included as well. Footprints for 0603 resistors and capacitors are also included on every analog channel, allowing the user to create a customized voltage divider if needed.

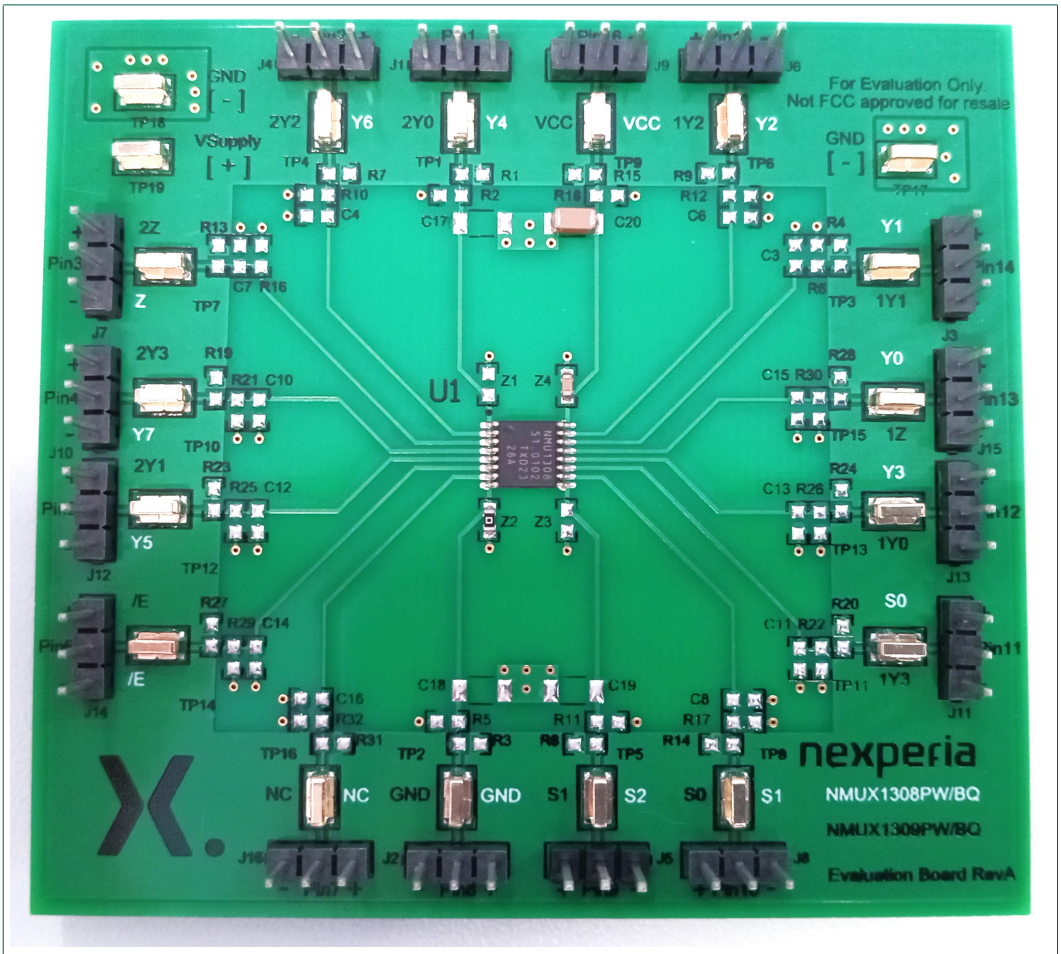

Fig. 1. NMUX1308; NMUX1309 Evaluation Board

NMUX1308; NMUX1309 device background

The list below gives a summary of the key parameters and most important features of the NNMUX1308; NMUX1309 devices.

- Wide operating range: 1.5 V to 5.5 V
- Control signal pins maintains 1.8 V logic compatibility at higher V_{CC}
- Rail-to-Rail operation on analog signal pins
- Powered-down protection: no ESD path from I/O pins to V_{CC}
- Injection current control: coupling does not exceed 1 mV/mA
- Fail-Safe logic on control signal pins
- Pin compatible with industry standard 74HC4051/74HC4052 and 74HC4851/74HC4852 analog switch products
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

2. Hardware setup

Higher level configuration summary:

- Test points on V_{CC}, GND, Yn (1Yn, 2Yn), Z (nZ), and Sn pins
- Passive footprints for customized divider circuit
- Selectable header shunts to connect inputs to V_{CC} or GND
- Board supports NMUX TSSOP16 or DHVQFN16 footprints.

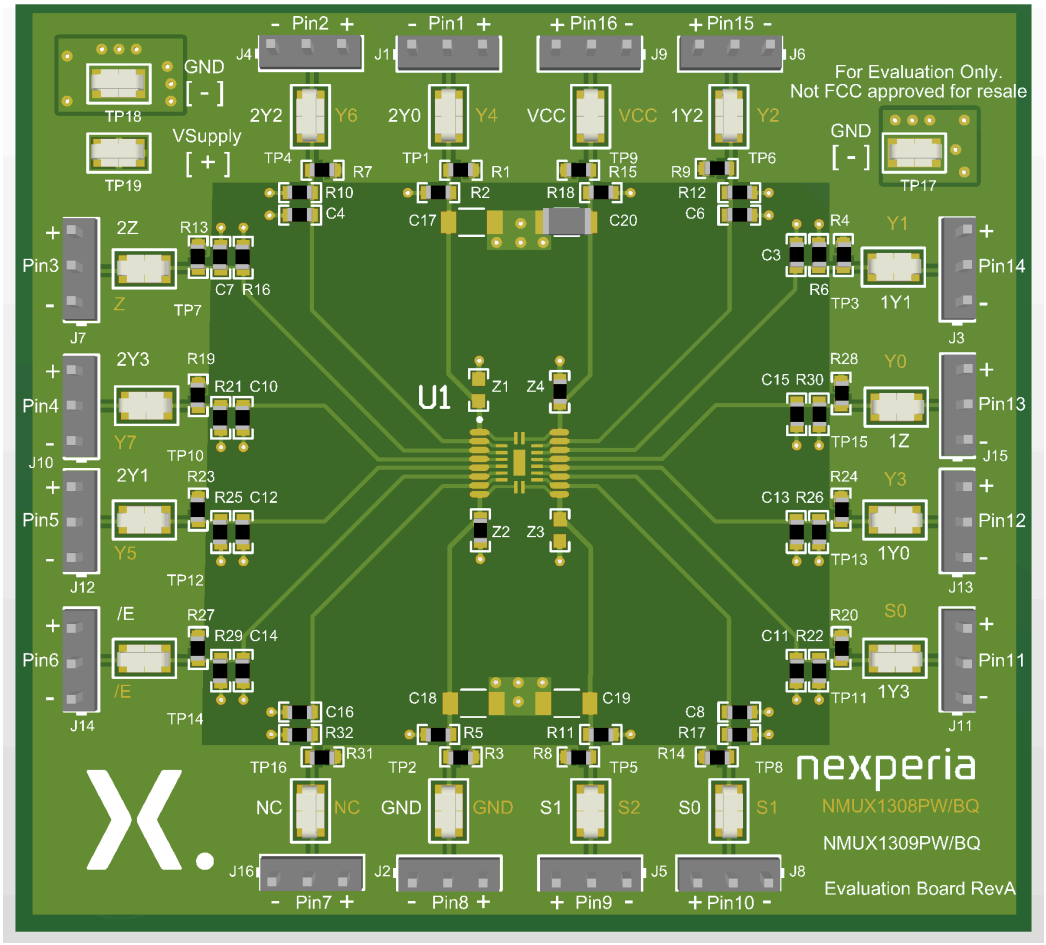

Fig. 2. 3D rendering of NMUX1308; NMUX1309 evaluation board

Typical connection is displayed in the 2D-rendered image, Fig. 3.

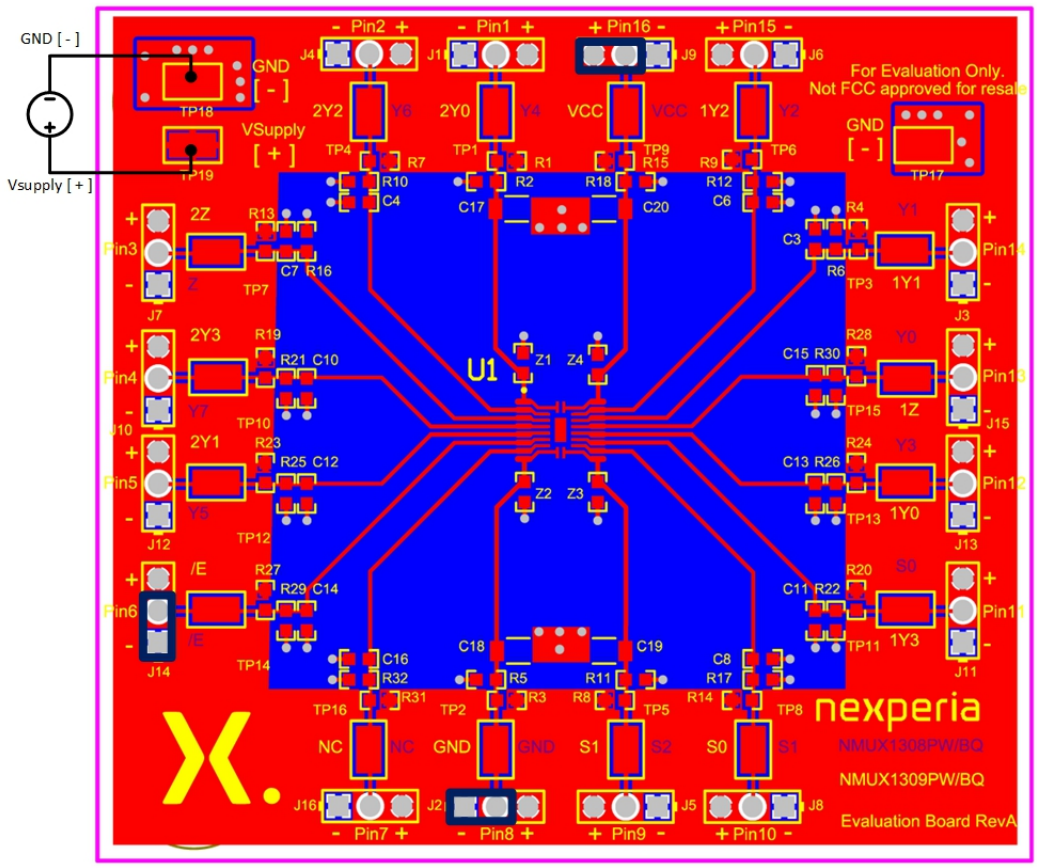

Fig. 3. 2D Rendering of NMUX1308; NMUX1309 evaluation board with default jumper settings

The proceeding section describes the EVB jumper and header description.

3. Test points V_{supply} [+] and GND [-]

TP19 (V_{supply} [+]) and TP17/TP18 (GND [-]) serve as the physical connection for the external supply. The top plane of the board, which is a ring in shape, connects to V_{supply} [+], while the bottom plane directly connects to the GND [-] test points. Device pins can connect to these planes by selecting the 2.54 mm shunt between their respective pin and '-' or '+' pin. By default the V_{CC} and GND EVB jumpers should connect to '+' and '-', respectively. This is shown in Table 1. A detailed description of the Header pinouts are listed in the tables presented below.

Table 1. Detailed description of the header pinouts

Net names	Header/Pin number	Description
V_{supply} [+]	TP19	External supply V_{CC} connection
GND [-]	TP17/TP18	External supply GND connection

Each pin of the device is brought out to a 3-pin header. The user can directly make connection to pin 2 of the headers or attach clips to its respective test point. Additionally, the V_{CC} and GND pins should be manually shunted to the V_{supply} [+] and GND [-] planes of the board. For default jumper settings, please refer to the image in Fig. 3.

The board provides two sets of silkscreen colors, allowing an easy way to reference either the NMUX1308 or NMUX1309 pin names.

Table 2. Detailed description of the header pinouts

Device pin number	Header connection	Test point clip label	NMUX1308 pin name	NMUX1309 pin name	2.5 mm shunt connection description
1	J1-2	TP1	Y4	2Y0	• 1-2 GND [-] • 2-3 V_{supply} [+]
2	J4-2	TP4	Y6	2Y2	• 1-2 GND [-] • 2-3 V_{supply} [+]
3	J7-2	TP7	Z	2Z	• 1-2 GND [-] • 2-3 V_{supply} [+]
4	J10-2	TP10	Y7	2Y3	• 1-2 GND [-] • 2-3 V_{supply} [+]
5	J12-2	TP12	Y5	2Y1	• 1-2 GND [-] • 2-3 V_{supply} [+]
6	J14-2	TP14	$\overline{E}$	$\overline{E}$	• 1-2 GND [-] • 2-3 V_{supply} [+]
7	J16-2	TP16	NC	NC	• 1-2 GND [-] • 2-3 V_{supply} [+]
8	J2-2	TP2	GND	GND	• 1-2 GND [-]
9	J5-2	TP5	S2	S1	• 1-2 GND [-] • 2-3 V_{supply} [+]
10	J8-2	TP8	S1	S0	• 1-2 GND [-] • 2-3 V_{supply} [+]
11	J11-2	TP11	S0	1Y3	• 1-2 GND [-] • 2-3 V_{supply} [+]
12	J13-2	TP13	Y3	1Y0	• 1-2 GND [-] • 2-3 V_{supply} [+]
13	J15-2	TP15	Y0	1Z	• 1-2 GND [-] • 2-3 V_{supply} [+]
14	J3-2	TP3	Y1	1Y1	• 1-2 GND [-] • 2-3 V_{supply} [+]
15	J6-2	TP6	Y2	1Y2	• 1-2 GND [-] • 2-3 V_{supply} [+]
16	J9-2	TP9	V_{CC}	V_{CC}	• 2-3 V_{supply} [+]

In addition to the NMUX1308; NMUX1309 PW and BQ packages, the EVB can universally evaluate any 16 pin PW or BQ device, such devices include 74HC4051/74HC4052 and 74HC4851/74HC4852. The generic footprint for U1 is shown in Fig. 4.

Note: The EVB can be universally used to evaluate any 16-pin (PW) or (BQ) packaged device. Z1, Z2, Z3, Z4 can be swapped for any arrangement of 0603 capacitors or 0 Ω resistors. For the NMUX1308/NMUX1309, Z4 and Z2 are set to a bypass capacitor and 0 Ω resistor, respectively.

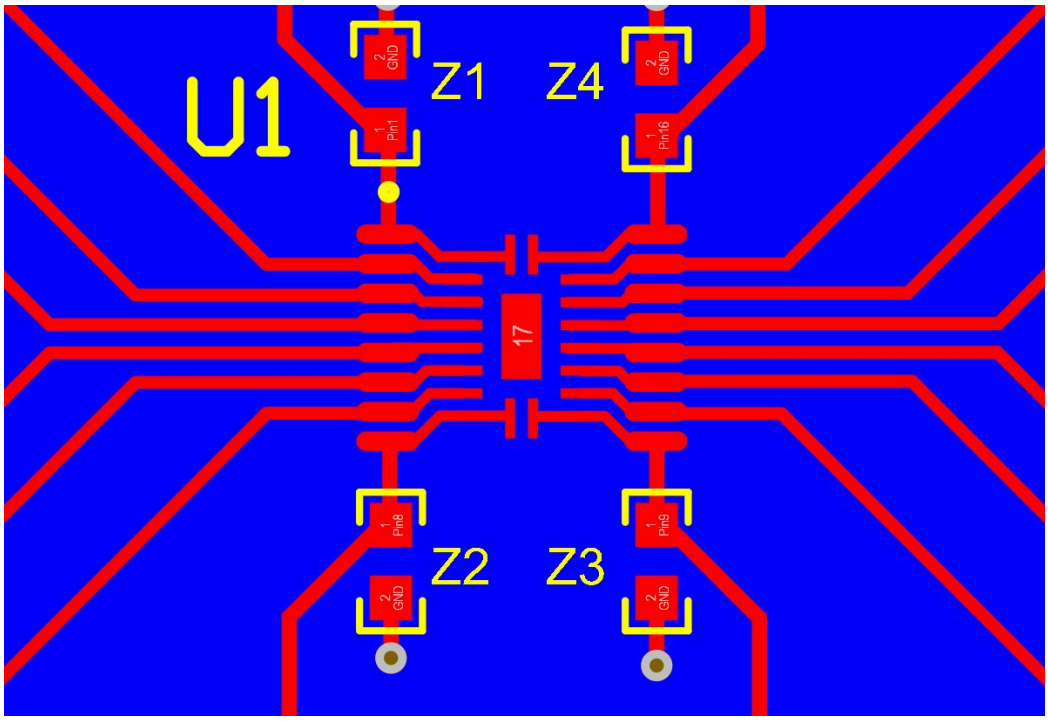

Fig. 4. 16 pin PW and BQ dual footprint

Each pin of the NMUX130x EVB includes one pull-up and pull-down resistor 0603 footprint so the user can populate a resistor divider in reference to V_{supply} [+]. This can be used to evaluate different nodal voltages at the input of the NMUX130x device. Additionally, 0603 ceramic capacitor footprints are also included in the case the user wishes to add capacitance to the signal net.

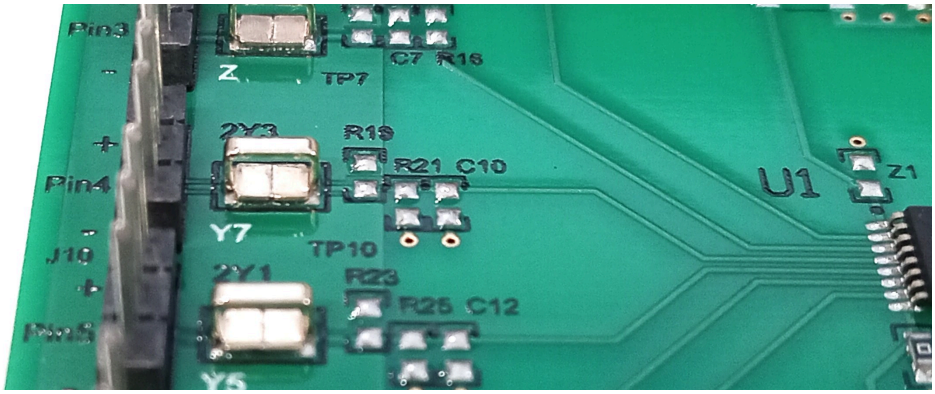

Fig. 5. Input pins passive footprints

4. Schematic diagram, Printed Circuit Board and Bill of Material

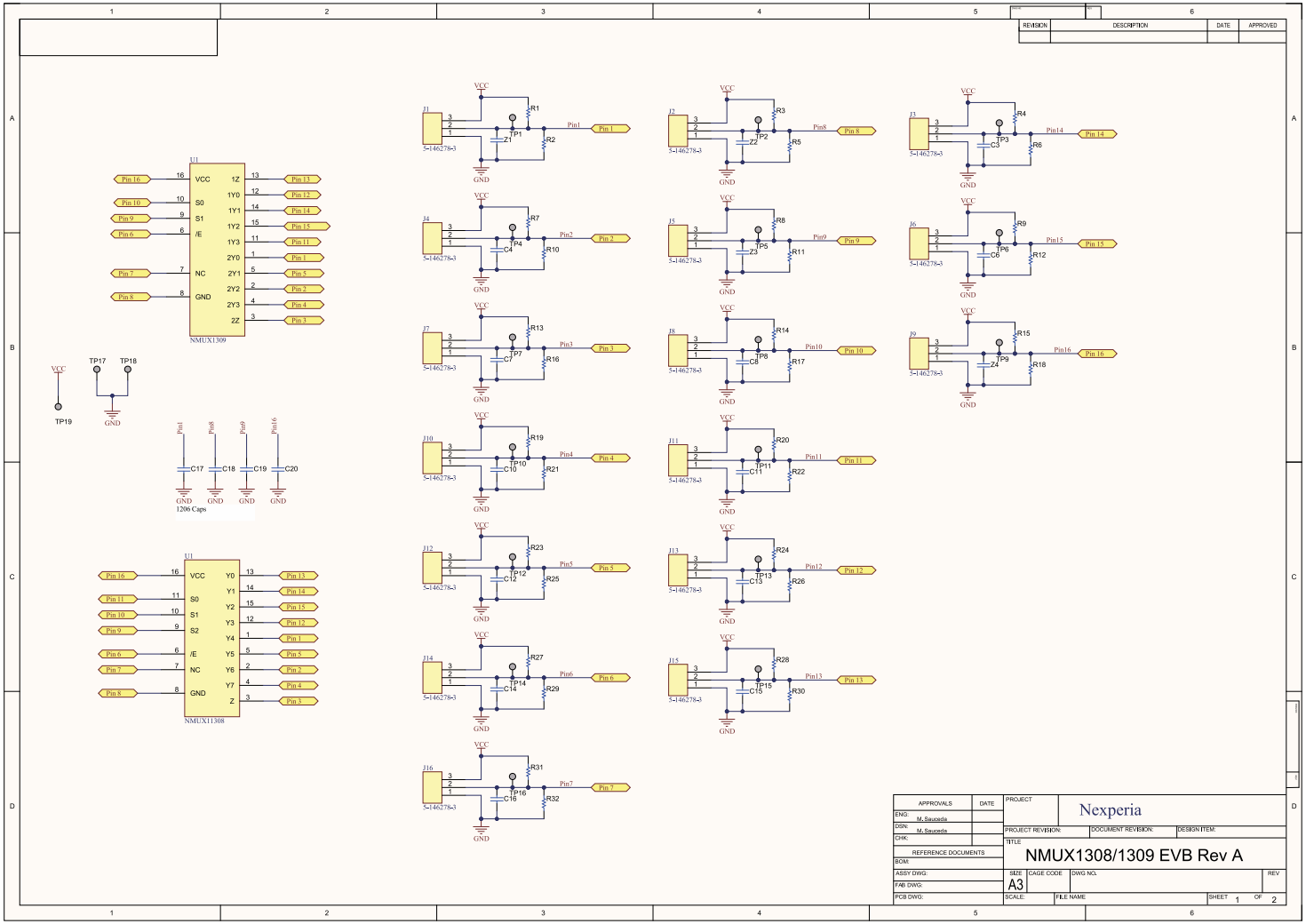

Fig. 6. Schematic diagram of NMUX1308; NMUX1309 evaluation board

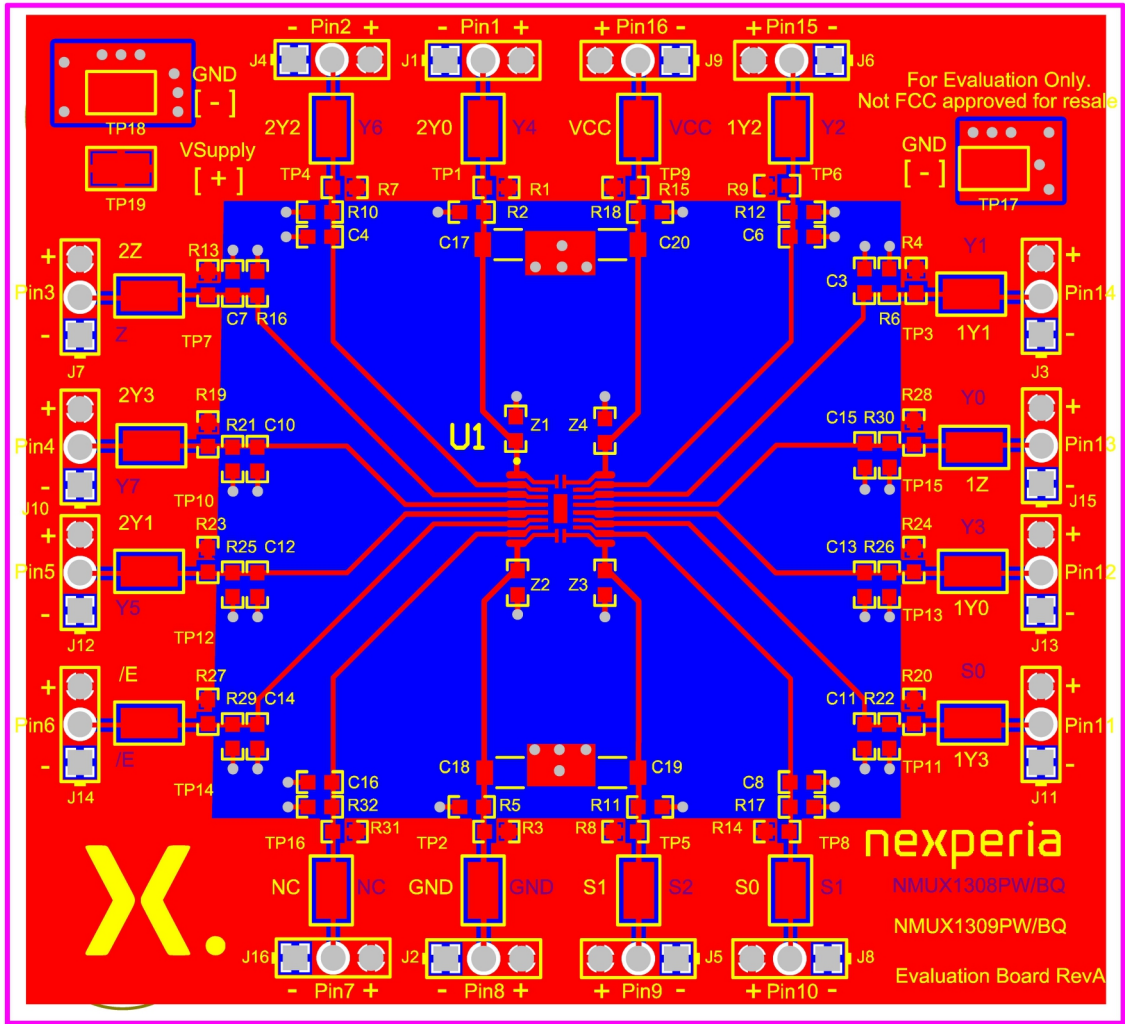

Fig. 7. Printed Circuit Board (PCB) layout top side

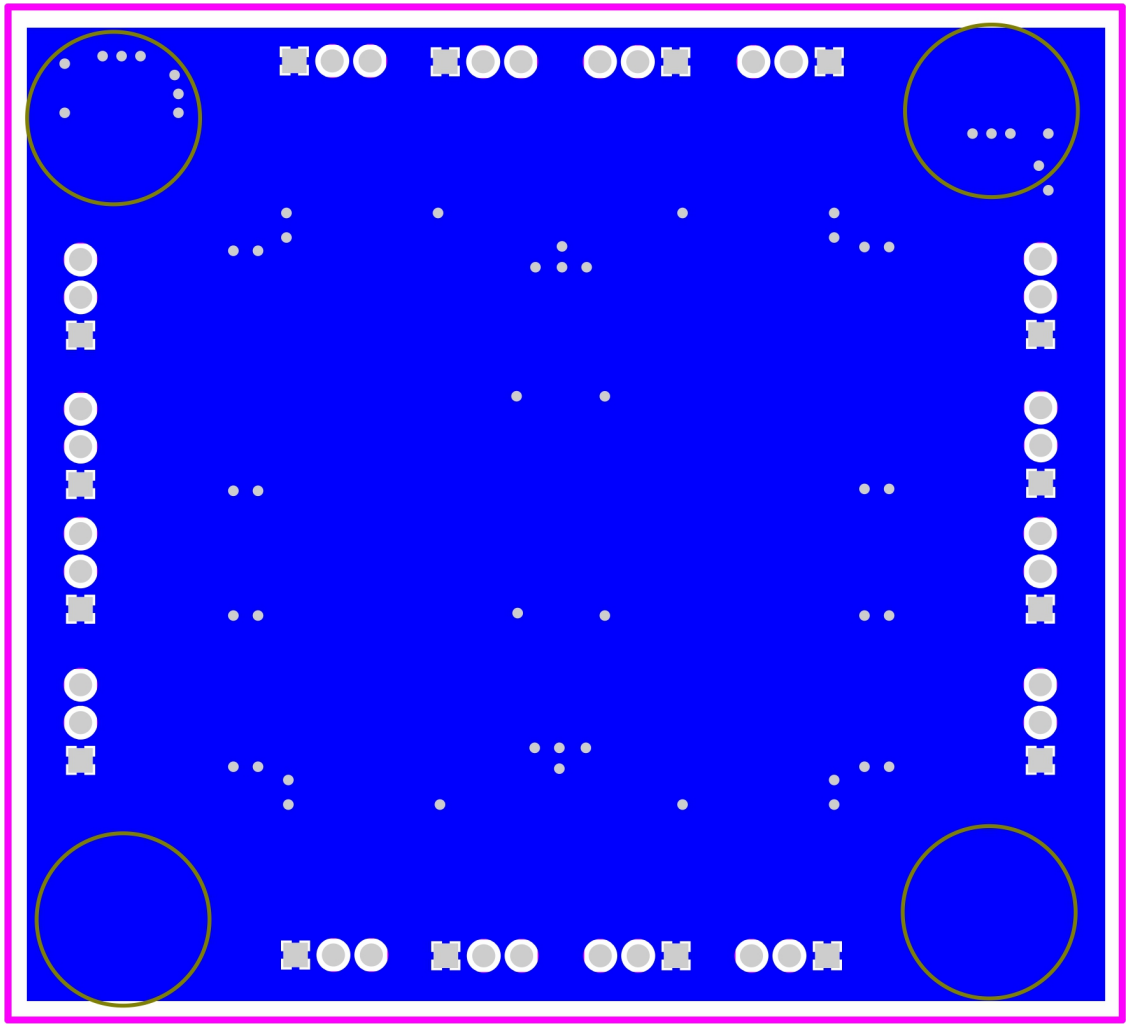

Fig. 8. Printed Circuit Board (PCB) layout back side

Table 3. Bill of Materials (BOM)

Part Number	Designator	Quantity
5019	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19	19
5-146278-3	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16	16
SJ-5303 (CLEAR)	H10, H11, H12, H13	4
GRM31CR71E106KA12L	C20	1
NMUX1308/1309	U1	1
RC0603JR-070RL	Z2	1
GCM188R71E105KA64D	Z4	1

5. Revision history

Table 4. Revision history

Revision number	Date	Description
UM90026 v.2	20240430	Section 3: First paragraph removed. (errata)
UM90026 v.1	20240118	Initial version

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